"Techniques for Producing 3D ICs with High-Density Interconnect"

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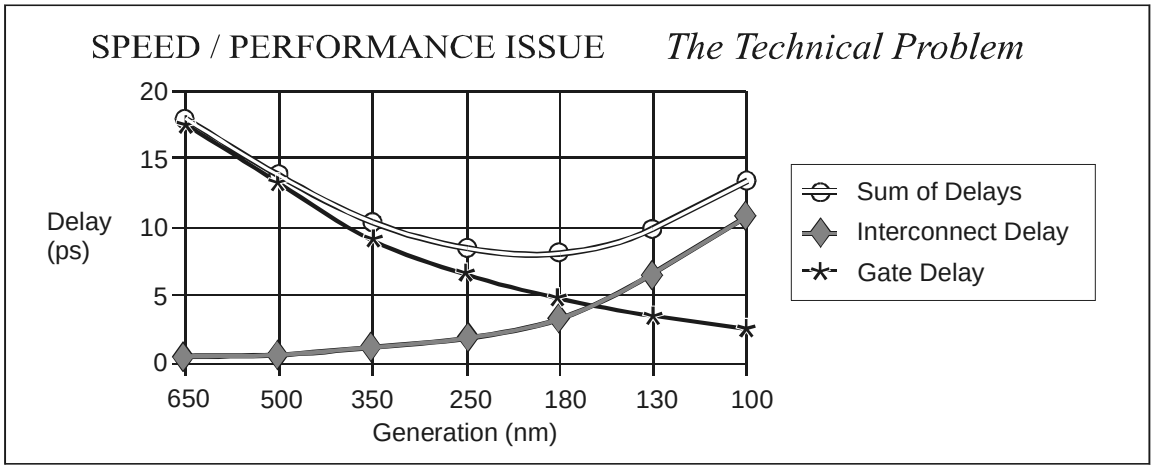
Abstract
It has been assumed that Moore's Law will end when smaller transistors no longer function, or perhaps when small-scale lithography becomes impractical. Recent events and the comments of industry leaders suggest a different scenario: perhaps Moore's Law ends when interconnect limitations collide with development costs and design complexities. These three factors – interconnect, cost, and complexity – are fast becoming the true limitations on the next generation of semiconductors. Cost and complexity have multiple avenues to a solution, 3D integration being one such avenue. But for interconnect, perhaps only 3D integration can mitigate the fundamental physics problems.

Introduction
Today's semiconductor industry faces ever-increasing challenges to producing the next generation of advanced components. The cost of component development is nearing $100M; a next generation foundry may hit $5B; and a huge new problem has emerged: the interconnect, which has mostly been ignored, now threatens Moore's Law.

"$3x10^8$ meters per second – it's not just a good idea, it's the Law!" And so are the effects of interconnect on the speed of complex devices. Transistors continue to improve in performance at smaller scales, but the wiring which connects them peaked in efficiency somewhere between 130nm and 90nm. In fact, the performance improvement gained in transistor scaling is insignificant compared to the negative effects of interconnect scaling. The only workable way to achieve real improvement in semiconductor systems is by reducing the average length of the interconnecting wire.



(Figure taken from "Heterogeneous Integration" *Tech Trend Notes*, September 2003)

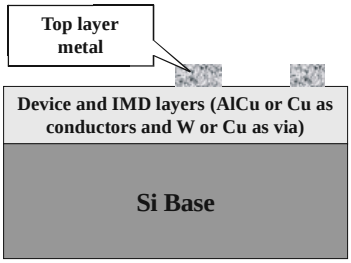
Any successful approach to 3D integration must address both technical and economic issues. This can be done by forming 3D circuits with direct copper interconnect and by incorporating fine-grained repair and redundancy. True 3D integration requires very high density vertical interconnects to overcome the drag created by wire scaling. This is possible with a new vertical interconnect technology that achieves micron scale connection with high reliability. The ability to create 3D ICs creates a desire to build much larger semiconductor systems. This, in turn, raises the specter of significant yield difficulties. The yield problem can be solved by improved repair and redundancy schemes that are enabled by the same wiring improvements that enable 3D integration.

Tezzaron's 3D Solution

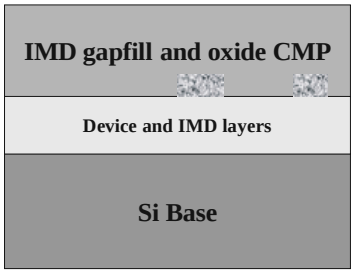
Tezzaron's first key breakthrough in 3D development was the Super-Via™ - a vertical copper structure that adapts standard process flow wafers to Tezzaron's 3D stacking process. Super-Vias can be post processed into any wafer merely by adding copper metallization and additional dielectrics, so they do not require a full manufacturing line or direct involvement of an outside foundry. Further, the Super-Via interconnect provides alignment marks, thinning control, interconnect, and bonding surfaces in a single structure. It further adds intrinsic cooling capabilities with its vertical copper structures.

As a side note, copper interconnect was not the first choice. Aluminum was experimented with at length and proved non-viable for a number of reasons. Copper proved to be nearly ideal, for the same reasons that have led to its use in a wide variety of commercial metal to metal bonding processes.

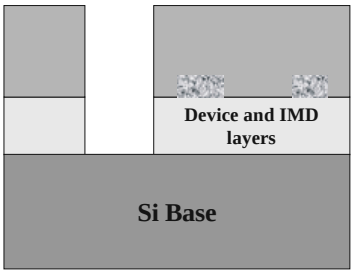
The process flow for Super-Via interconnect is straightforward and uses traditional equipment. Perhaps the only unusual piece of foundry equipment in the process is the EVG (Electronic Visions Group) aligner/bonder, which is not found in most process flows, but is in widespread use for MEMS and the creation of unique substrates. The following sequence provides a simplified description of Tezzaron's 3D construction process:



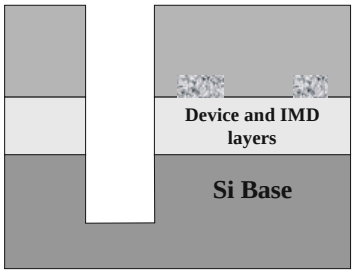
1. The product wafer is fabricated with devices and multiple metal layers.



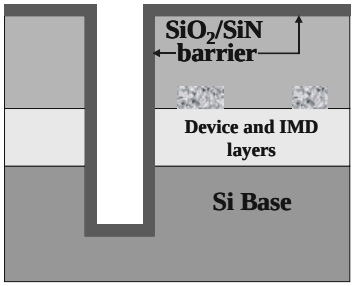
2. Inter-Metal Dielectric (IMD) is deposited on the wafer by HDP, then planarized by oxide CMP.



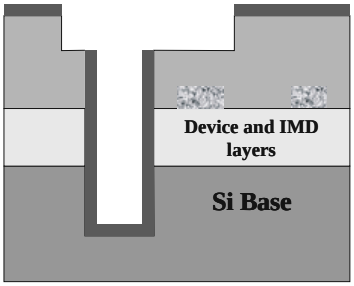
3. A Super-Via™ (2 to 4 µm) is masked, then the whole dielectric stack is etched.



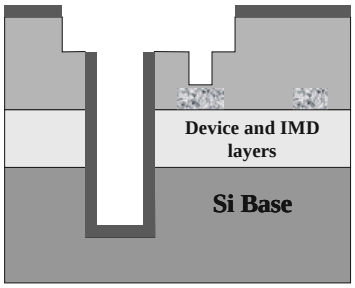
4. The Si base is etched to a depth of from 4 to 9 µm, with part of the IMD as the hard-mask.



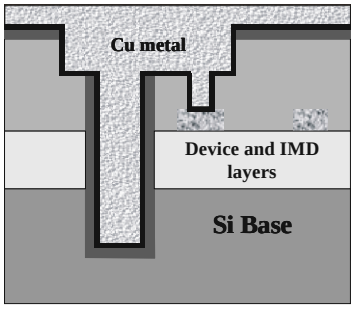
5. An oxide layer and an SiN layer are deposited, each ~0.05 to 0.1 µm. The SiN acts as a polish/etch stop and as additional protection against Cu diffusion into the Si.



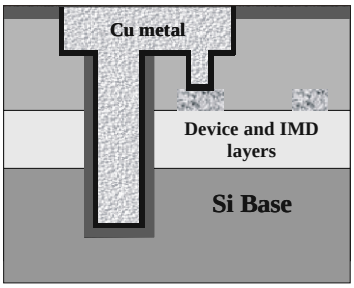
6. Trenches for future wafer-to-wafer bonding are masked and then etched (trench first dual damascene etching).



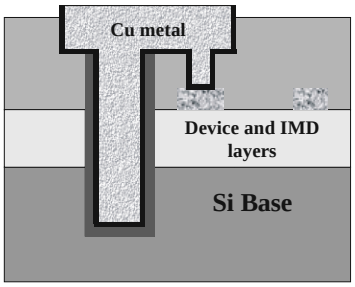
7. Another via is masked and etched to electrically connect the future bonded wafers.



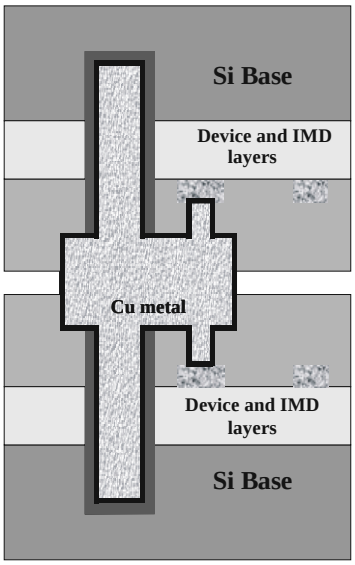
8. A Ta or TaN barrier and Cu seed are deposited, followed by Cu Electrochemical Plating (ECP).



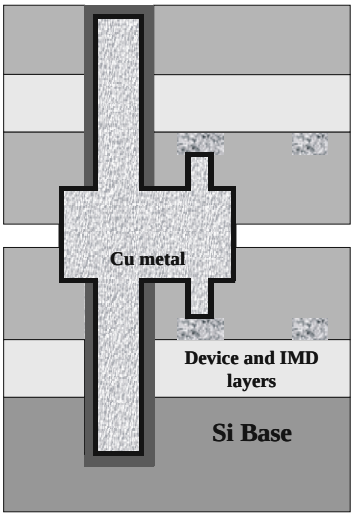
9. Excess Cu and Ta are removed by CMP.



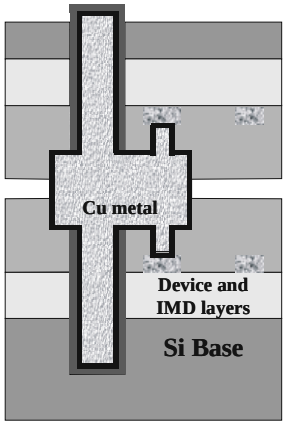
10. Either the trench dielectric is recessed or else the Cu pad is elevated by selective electroless deposition.



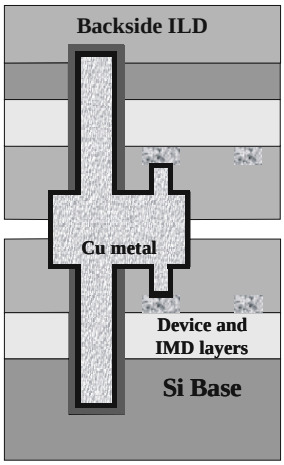
11. Two wafers are thermal diffusion bonded, face-to-face.



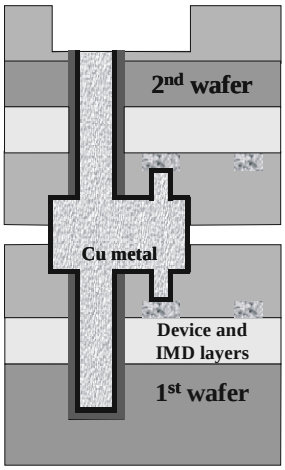
12. The base Si on one wafer is thinned by grinding and CMP. The alignment plug is both a stop-layer for the Si thinning and an alignment mark for later wiring.



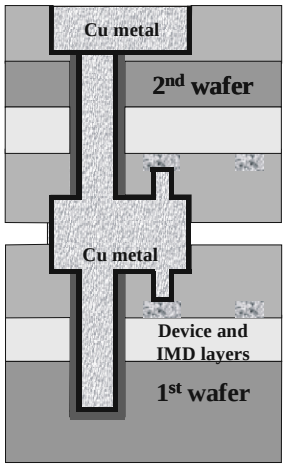
13. After grinding and CMP, the Si is further recessed by chemical etch (not more than 1μm).



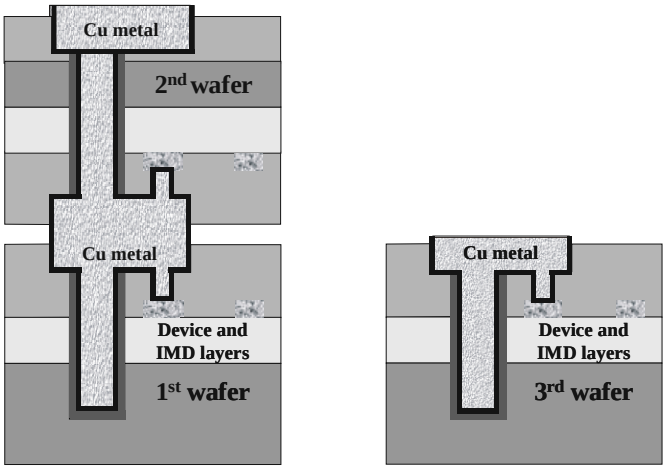
14. A layer of PECVD SiO_2 is deposited on the backside of the wafer to avoid contamination of Si during subsequent Cu metallization.



15. The same pad mask is used to pattern the backside dielectric, forming exactly the same trench pattern as the front side.



16. Standard Cu metallization is used with a Ta or Ta/TaN barrier followed by Cu seed, Cu ECP, and finally Cu CMP.



17. Again, either the trench dielectric is recessed or the Cu pad is elevated by selective electroless deposition

Since the early development and success with the Super-Via flow, Tezzaron has been developing a new second generation of interconnect. This second generation interconnect does involve the primary wafer foundry, but it adds more design flexibility while drastically decreasing the 3D interconnect footprint. As can be seen in the table below, Tezzaron's interconnect methods enable high-density interconnect for true circuit-level 3D integration.

	Super-Via™	2nd Generation	Face-to-Face
Size	4.0 μ x 4.0 μ	1.2 μ x 1.2 μ	1.7 μ x 1.7 μ
Minimum Pitch	6.08 μ	<4 μ	2.4 μ (1.46 μ)
Feed-Through Capacitance	7 fF	2-3 fF	<<
Series Resistance	<0.25 Ω	<0.35 Ω	<

The Big Picture

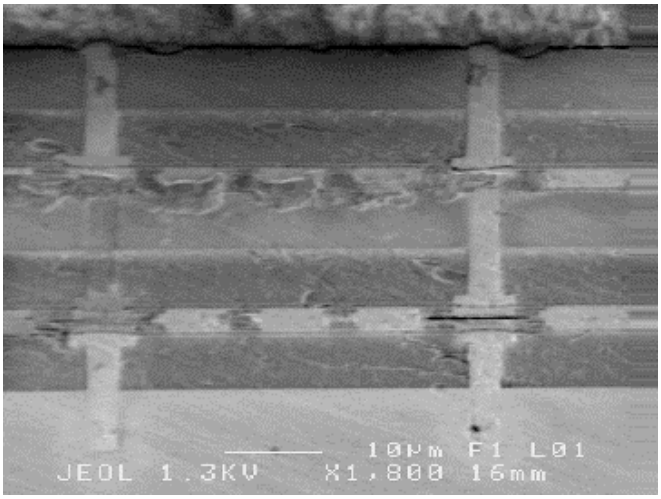
There are other requirements that bear mentioning. While a workable commercializable process flow is mandatory, other very significant issues must also be addressed. These include yield management and tool flow.

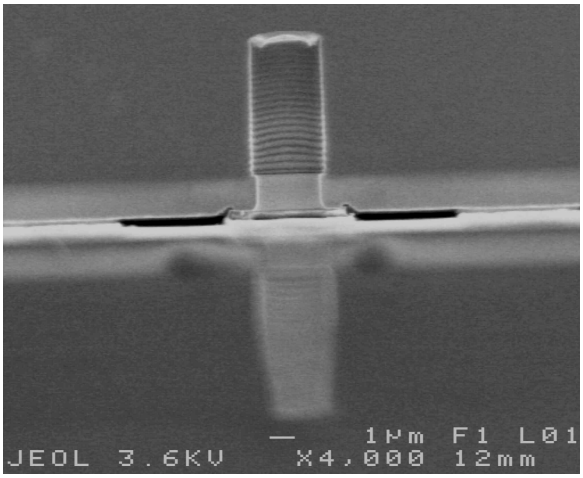
Tezzaron has used a tool flow based on the standard Cadence toolset. Additional scripts and methodologies were required, but these were mostly straight-forward extensions of existing concepts. Although this toolset provides the basics, such as DRC and LVS, there is still much work to be done. Advances are needed in the synthesis and place-and-route before 3D is as good as 2D in these areas.

The issue of yield management is a larger concern. If the yield of a circuit in 2D is, say, 80%, then in 3D that same circuit's yield would still be about 80%. And while 3D can provide this solution and give the benefits of lower power and enhanced speed, most users would want more. Instead of dividing a single $100mm^2$ die into, say, four $25mm^2$ dice for 3D interconnection, users really want four $100mm^2$ dice interconnected in 3D. In this case, the yield approaches that of a single $400mm^2$ die. A more robust approach to yield management is required. For most regular structures, such as memories and FPGAs, redundancy works well. The penalty, other than additional silicon area, is generally paid in terms of speed and increased routing congestion. It is beyond the scope of this paper to detail the complete solution, but one can quickly grasp that the inherent benefits of the 3D interconnect, more routability and closer proximity to a larger number of transistors, provide the fundamentals to solving the yield issue. The key to yield lies not in eliminating the bad transistors, but in providing fast and easy access to the good transistors.

The Results

Tezzaron has stacked a variety of wafer types, including SOI and bulk wafers, using both the original Super-Via and the new enhanced second generation process flows. Experiments have shown that the 3D-enabled wafers can be thinned to as little as a few microns. They can be stacked with sub-micron alignment. The bonded wafers have a Cu-Cu bond strength that is greater than required and actually stronger than the Cu-SiO_2 interface. Also, the interconnected wafers can be handled in a normal fashion without special handlers or precautions. The transistors on the stacked, bonded, and thinned wafers were shown to have no discernable performance differences from their original 2D form.





Conclusions

Tezzaron has demonstrated its 3D process flow on a wide variety of test vehicles, consistently aligning 200mm wafers with sub-micron accuracy, thinning wafers in the 3D stack with sub-micron thickness control, and producing up to four-layer wafer stacks.