2.5/3D Integrated Circuit Technology

Capabilities and Industry Readiness

Robert Patti, CTO

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Span of 3D Integration

Packaging

3D Through Via Chip Stack

IBM/Samsung

Tezzaron 3D-ICs

100-1,000,000/sqmm

1000-10M Interconnects/device

Peripheral I/O

- Flash, DRAM
- CMOS Sensors

1s/sqmm

100,000,000s/sqmm

Transistor to Transistor

Ultimate goal

Wafer Fab

Tezzaron Semiconductor

09/04/2014
Why 3D? – Expiring Economics

The next node may not crossover

Source: AMD

AMD 2014 3D-ASIP
Why 3D? – Expiring Economics

Gate Costs for Bulk CMOS and FinFET

Source: International Business Strategies, Inc.

Tezzaron Semiconductor
Why 3D? – Apples & Oranges
HMC Micrograph
Gen4 “Dis-Integrated” 3D Memory

2 million vertical connections per layer per die

I/O layer contains: I/O, interface logic and R&R control CPU. 65nm node

Better yielding than 2D equivalent!

DRAM layers 4xnm node

Controller layer contains: sense amps, CAMs, row/column decodes and test engines. 40nm node
# 3D Interconnect Characteristics

<table>
<thead>
<tr>
<th></th>
<th>SuperContact™ I 200mm Via First, FEOL</th>
<th>SuperContact™ IV 200mm Via First, FEOL</th>
<th>SuperContact™ V 300mm Via F/L, FEOL</th>
<th>SuperContact™ VI 300mm Via F/L, FEOL</th>
<th>Interposer TSV</th>
<th>Bond Points</th>
<th>Die to Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong> L X W X D</td>
<td>1.2 µ X 1.2 µ X 6.0µ</td>
<td>0.6 µ X 0.6 µ X 2µ</td>
<td>1.2 µ X 1.2 µ X 6µ</td>
<td>0.8 µ X 0.8 µ X 6µ</td>
<td>10 µ X 10 µ</td>
<td>1.2 µ X 1.2 µ</td>
<td>2.5 µ X 2.5 µ</td>
</tr>
<tr>
<td><strong>Material</strong></td>
<td>W in Bulk</td>
<td>W in SOI</td>
<td>W in Bulk</td>
<td>W in Bulk</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
</tr>
<tr>
<td><strong>Minimum Pitch</strong></td>
<td>&lt;2.5 µ</td>
<td>1.2 µ</td>
<td>2.4 µ</td>
<td>1.6 µ</td>
<td>30 µ</td>
<td>2.4 µ</td>
<td>5 µ</td>
</tr>
<tr>
<td><strong>Feedthrough Capacitance</strong></td>
<td>2fF</td>
<td>0.2fF</td>
<td>1.5fF</td>
<td>1.2fF</td>
<td>150fF</td>
<td>&lt;&lt;</td>
<td>&lt;25fF</td>
</tr>
<tr>
<td><strong>Series Resistance</strong></td>
<td>&lt;1.5 Ω</td>
<td>&lt;1.75 Ω</td>
<td>&lt;2.0 Ω</td>
<td>&lt;3.0 Ω</td>
<td>&lt;0.5 Ω</td>
<td>&lt;</td>
<td>&lt;</td>
</tr>
</tbody>
</table>

**Small fine grain TSVs are fundamental to 3D enablement**
Tiny, Common, Cheap, Fast and…

10µ Diameter Copper TSV

1µ Diameter Tungsten SuperContact

Routable
A Closer Look at Wafer-Level Stacking

Dielectric (SiO2/SiN)
Gate Poly
STI (Shallow Trench Isolation)
W (Tungsten contact & via)
Al (M1 – M5)
Cu (M6, Top Metal)

“SuperContact”
Next, Stack a Second Wafer & Thin:
Stacking Process Sequential Picture

Two Wafer Align & Bond → Coarse Ground → Fine Ground

→ After CMP → Si Recessed

High Precision Alignment
Misalignment=0.3μm

Top wafer

Bottom wafer
Then, Stack a Third Wafer:
Finally, Flip, Thin, & Pad Out:

This is the completed stack!
3D Devices

Fig. 3. Surface of the “baby” pixel sensors with Sn-Pb deposited.

Fig. 4. VIPIC1 with flip-chip bonded “baby” pixel sensor.

Fig. 5. Transmission radiogram of a small W mask (2.5×2.5 mm$^2$) placed atop of the sensor back-side illuminated and fully depleted.

rows & cols skipped

ROIC area
TSV Insertion
Near End-of-Line TSV Insertion

TSV is 1.2µ Wide and ~10µ deep

5.6µ

2x, 4x, 8x Wiring level ~.2/.2µm S/W
2.5/3D Circuits

IME A-Star / Tezzaron Collaboration

Active Silicon Circuit Board

2 Layer Processor

3 Layer 3D Memory

μBumps

C4 Bumps

Die to Wafer Cu Thermal Diffusion Bond

Solder Bumps

Organic Substrate

Tezzaron Semiconductor

09/04/2014
Wafer-scale FPA
Luxtera 2.5D Photonic Data Pump

- 2.5pJ/bit power
- Bare metal protocol
  - Ultra low latency
  - Protocol agnostic
- 8 core Fiber
- 25Gb SERDES or 3.125Gb interface
- Self-calibrating self-tuning
- >1.6Tb/s payload
Mixed CMOS-3/5 100mm InP/CMOS

- GaN
- 3D CMOS/InP/GaN
- Graphene
Cooling Block Illustrations
“5.5D” Systems

- **SIP/SSIP**
  - Power Conversion
  - Cooling
  - Photonics

- **Optimization**
  - Extending to power

- **Mixed PCB/IC Metaphor**

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- **Decoupling and power supply passives**
- **Board to Board ~400 pin 5 mm height connector**
- **Full reticle footprint (28x24 mm)**
- **Die footprint**
  - HUBs (20x25 mm)
  - CPU(s) (20x25mm or 20x12mm)
- **Photonic Interfaces**
  - 2 x 2 x 1.6Tb links
- **SICB (silicon interposer 26x44mm)**
- **Stacked device**
  - CPU
  - NHub
  - MHub
- **32GBytes 4TByte/s Bandwidth**
- **Complete system**
  - 20TFlops
  - 200G packets/s
  - 16 x 10 Tb links
  - ~1200W

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Tezzaron Semiconductor
Package Floor Plan

- Power Regulator components
- Power Regulator components

Mem Stack 1
- 70x184 bump pitch
- 140 x 184 CuP pitch for power
- 384 sig 8 rows Wide Port

Mem Stack 0
- 70x184 bump pitch
- 140 x 184 CuP pitch for power

MHUB
- 384 sig 1 row maint

SiCB
- serdes
- serdes
- serdes

BGA package

DiRAM4™
- 12.98 mm

MSyPort™
- 13.54 mm

DiRAM4™
- 12.98 mm

6L Ceramic Substrate
- 45 mm Max

Tezzaron Semiconductor
Tezzaron/Novati 3D Technologies

- “Volume” 2.5D and 3D
- Interposers
- Cu-Cu, DBI®, Oxide, IM 3D assembly
- 193nm, 248nm, I-Line Litho
  - 70nm PS
  - 35nm DP
- 90nm CMOS
- 200/300mm
- Avalanche, SPM
- Fab1 Class 10 68K sf
- Fab2 Class 100 12K sf
Fusion versus Bump Bonding

Grzegorz Deptuch
Fermi National Accelerator Laboratory

5.4×6.5 mm² VIPIC with 32×38 pixels detector bump bonded

34 μm thick VIPIC DBI bonded to 64×64 with pads on its back
ENC comparison: bump vs. fusion bonded

Grzegorz Deptuch
Fermi National Accelerator Laboratory
Signal amplitude comparison: bump vs. fusion bonded

Grzegorz Deptuch
Fermi National Accelerator Laboratory

Gain is higher for fusion bonded device

Amplitude for bump-bonded VIPIC
Amplitude for fusion bonded VIPIC

32×38 = 1216 pixels bump-bonded
Summary

• “One stop” 2.5/3D solution provider
• Open technology platform
• Volume 2.5D Si interposer production
• Volume 3D assembly
• TSV Insertion
• Silicon, 3/5 materials, carbon nanotubes

Sensors
  Computing
    MEMS
  Communications