Tezzaron SEMICONDUCTOR

A Perspective on Manufacturing 2.5/3D

Bob Patti, CTO

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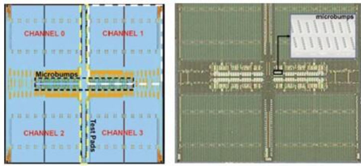
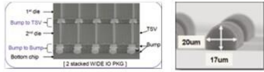
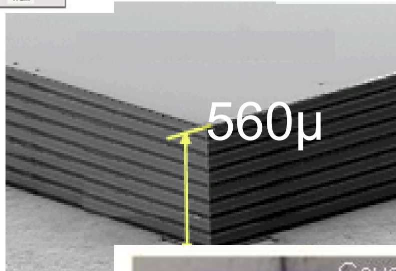
2.5 and 3D Opportunities & Goals

- Choices:
  - Interposers
    - Organic
    - Silicon
    - Glass
  - Chip stacking
  - Wafer to wafer
  - Die to wafer
- What do we want from doing this?
  - Performance
  - Power
  - Size
  - Cost ?
    - Near Term -- Only from the system

3D is Coming of Age







Samsung
Wide Bus DRAM

Micron
Wide Bus DRAM

Intel
CPU + memory

OKI
CMOS Sensor

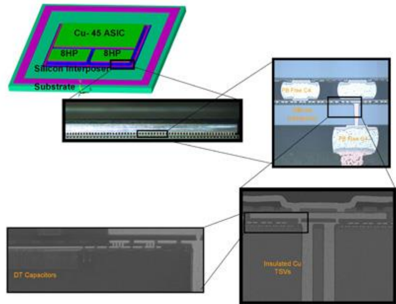
Xilinx
4 die 65nm interposer

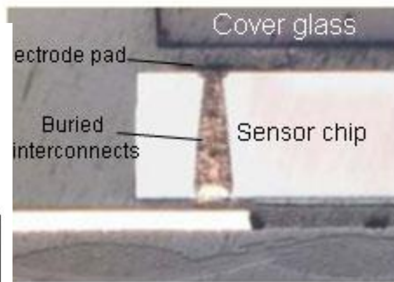
Raytheon/Ziptronix
PIN Detector Device

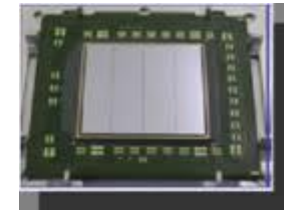
IBM
RF Silicon Circuit Board / TSV
Logic & Analog

Toshiba
3D NAND

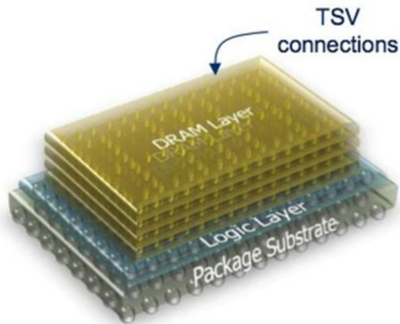
Samsung
22 layer 3D NAND

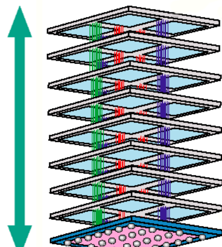


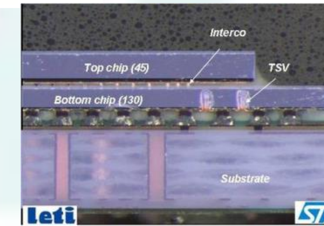


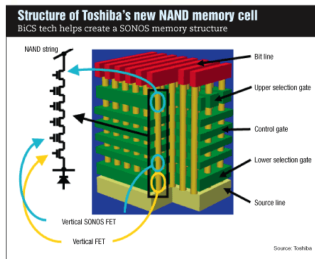


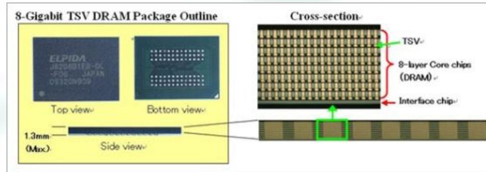
TSV connections











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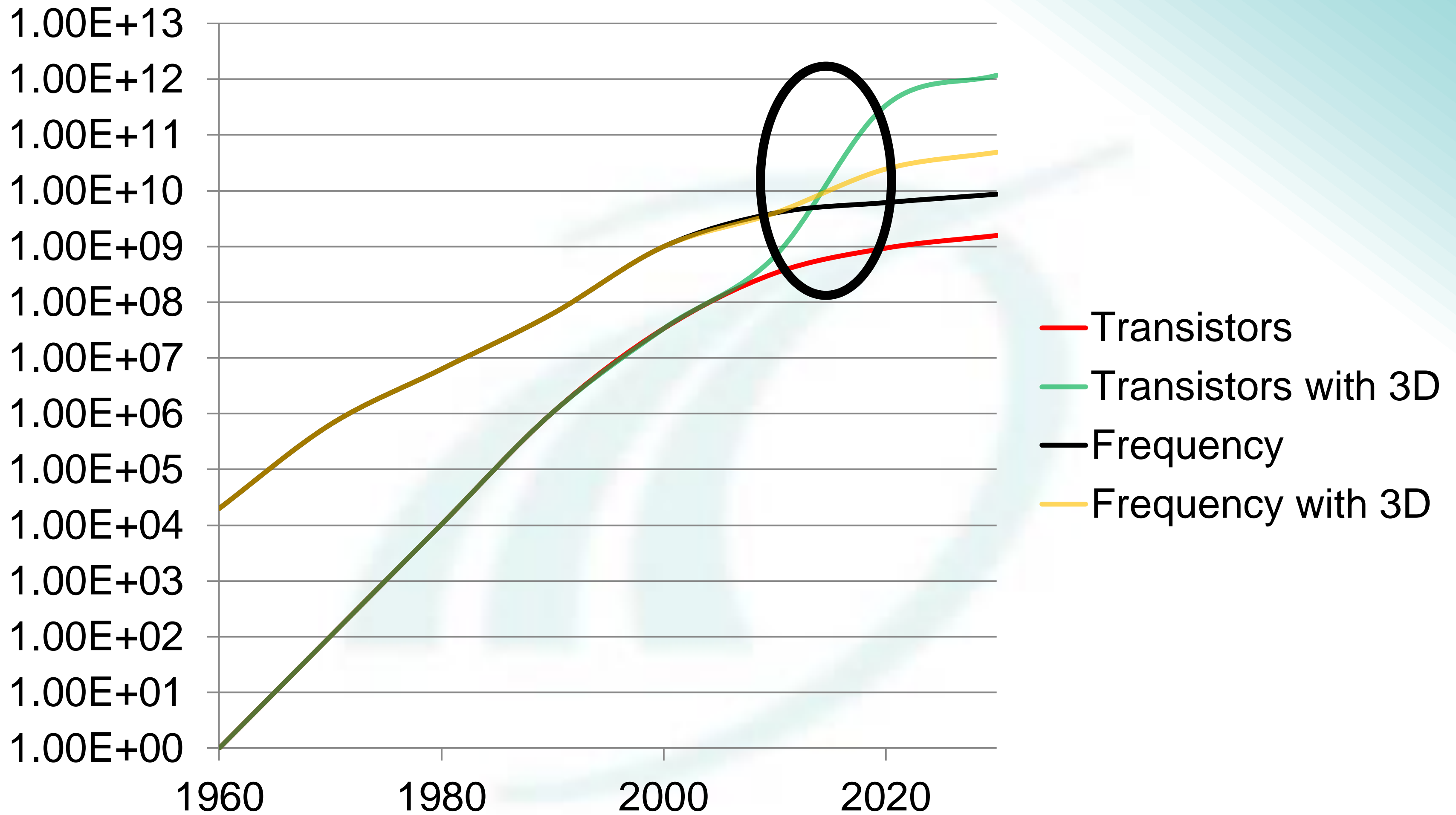
The Effect of 2.5/3D on Devices



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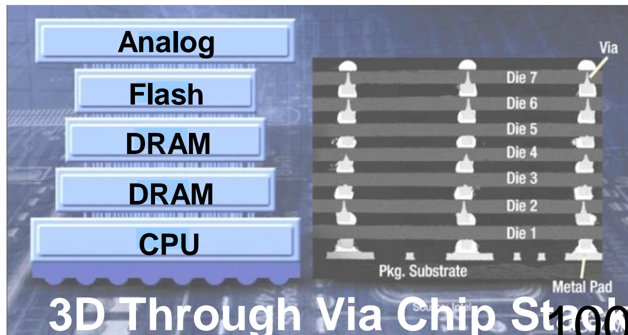
Span of 3D Integration

Rich and Varied Technologies

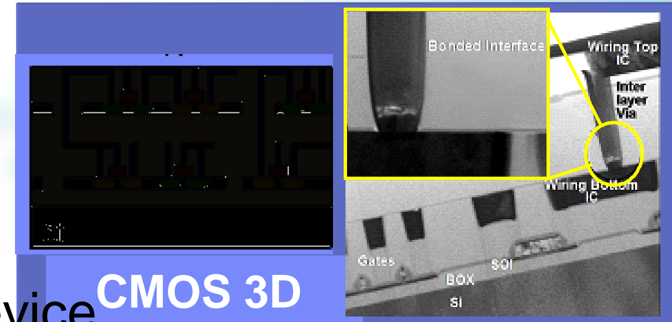
Packaging

Wafer Fab

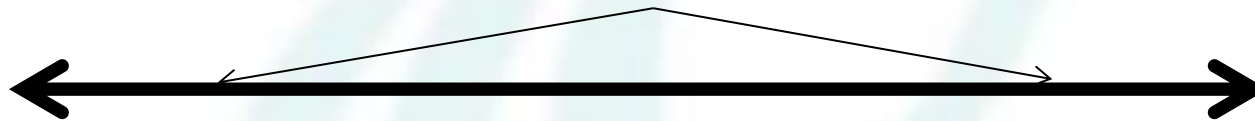


IBM/Samsung

Tezzaron
3D-ICs
100-1,000,000/sqmm
1000-10M Interconnects/device



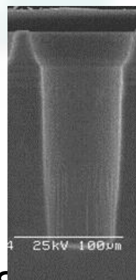
IBM



1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors



100,000,000s/sqmm

Transistor to Transistor

- Ultimate goal

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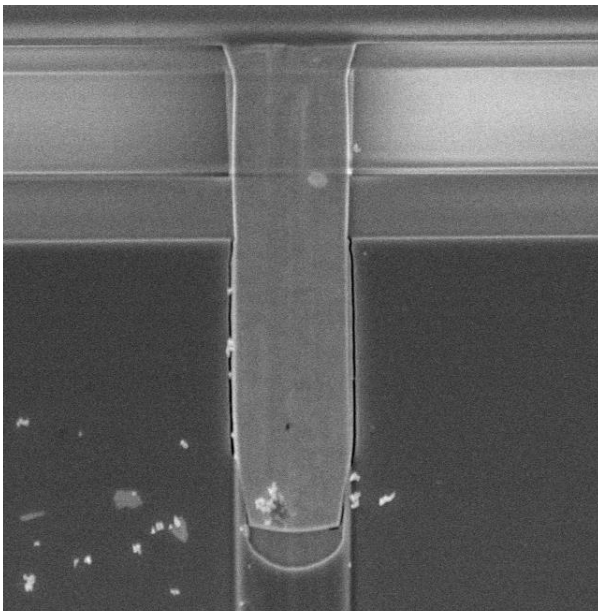
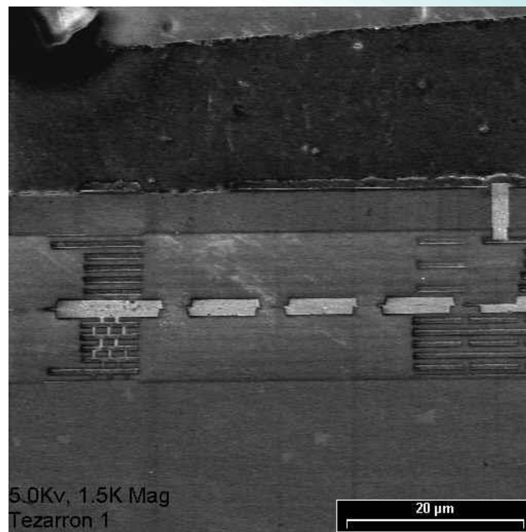
Technical Advances

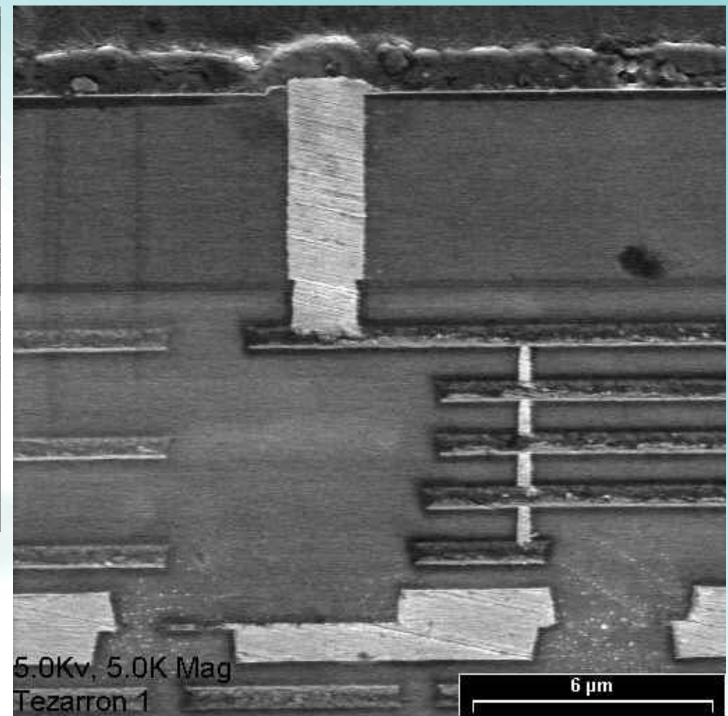
- TSV quality
  - Metrology
- Thinning control
  - TSV end point detection
- CAE tools
  - 3D DRC/LVS
  - Simulation of 3D devices
- Bond quality
- Designers have some handle on what can be done

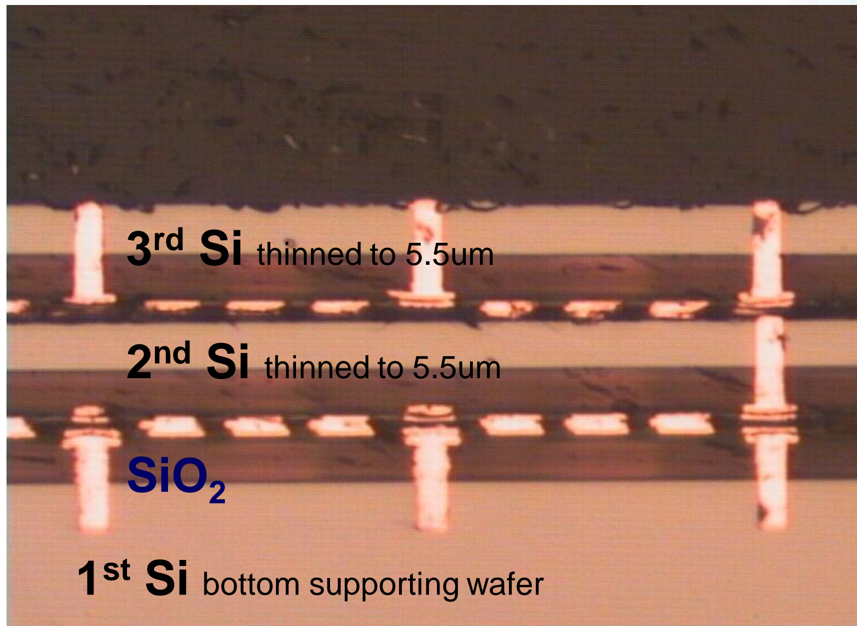
Industry Advances

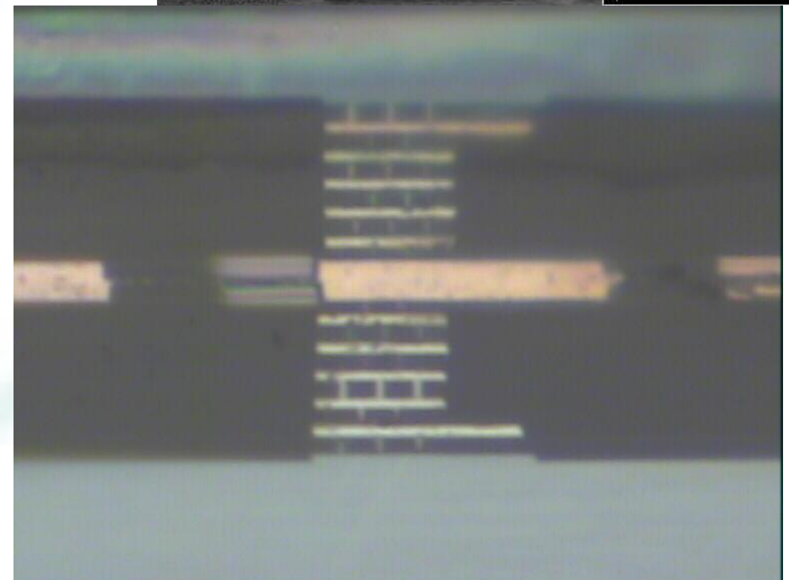
- There is an ecosystem
  - It is still young but it is in exponential growth mode
- Vendors are 3D aware!
  - TSV specific process hardware
  - 2.5D and 3D specific CAD
- It is not if – but when











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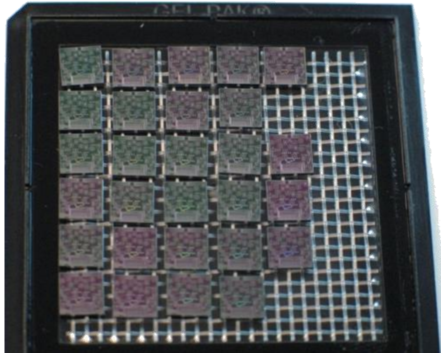

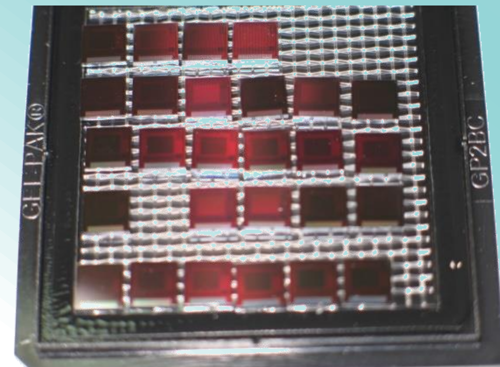

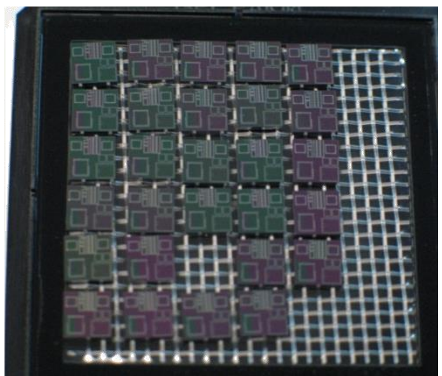

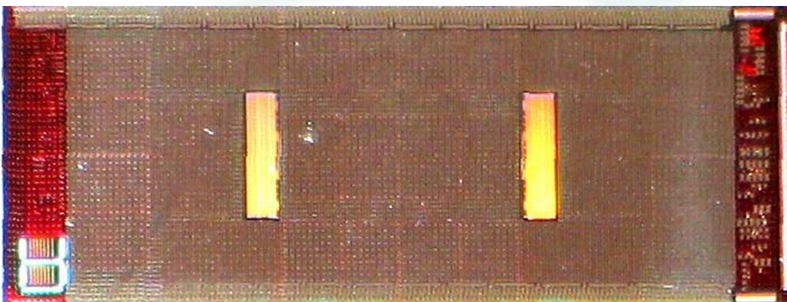

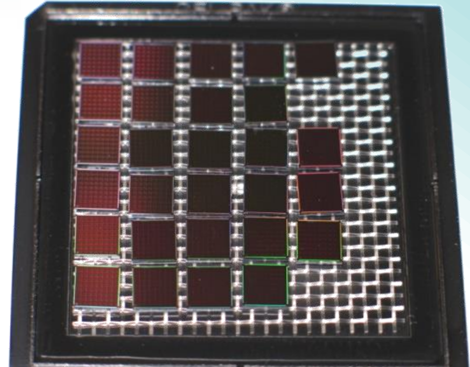

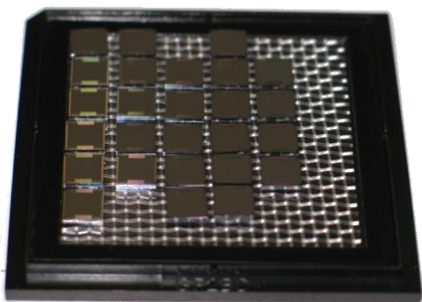

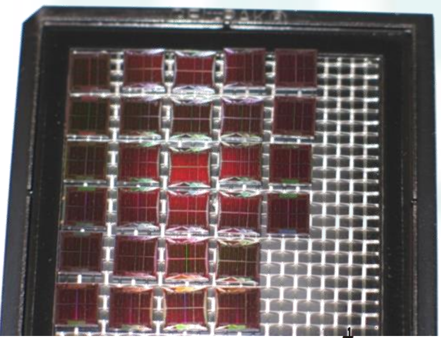

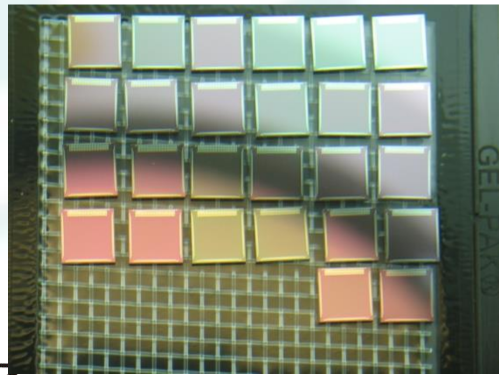

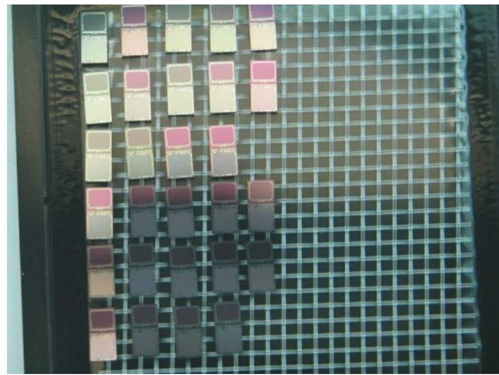

Tezzaron 3D Devices

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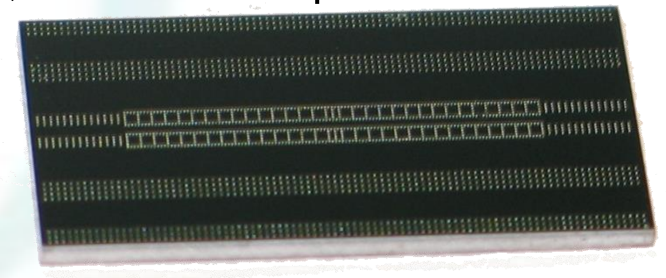
High Performance 3D Memory

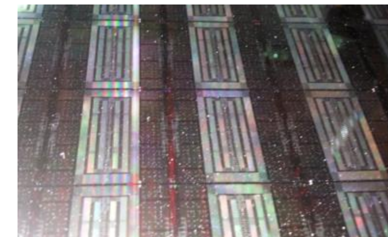
Octopus – Proof of Concept

- 1-4Gb
- 16 Ports x 128bits (each way)
- @1GHz
  - CWL=0 CRL=2 SDR format
  - 5ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >2Tb/s data transfer rate
- Max clk=1.6GHz
- Internally ECC protected, Dynamic self-repair, Post attach repair
- 115C die full function operating temperature

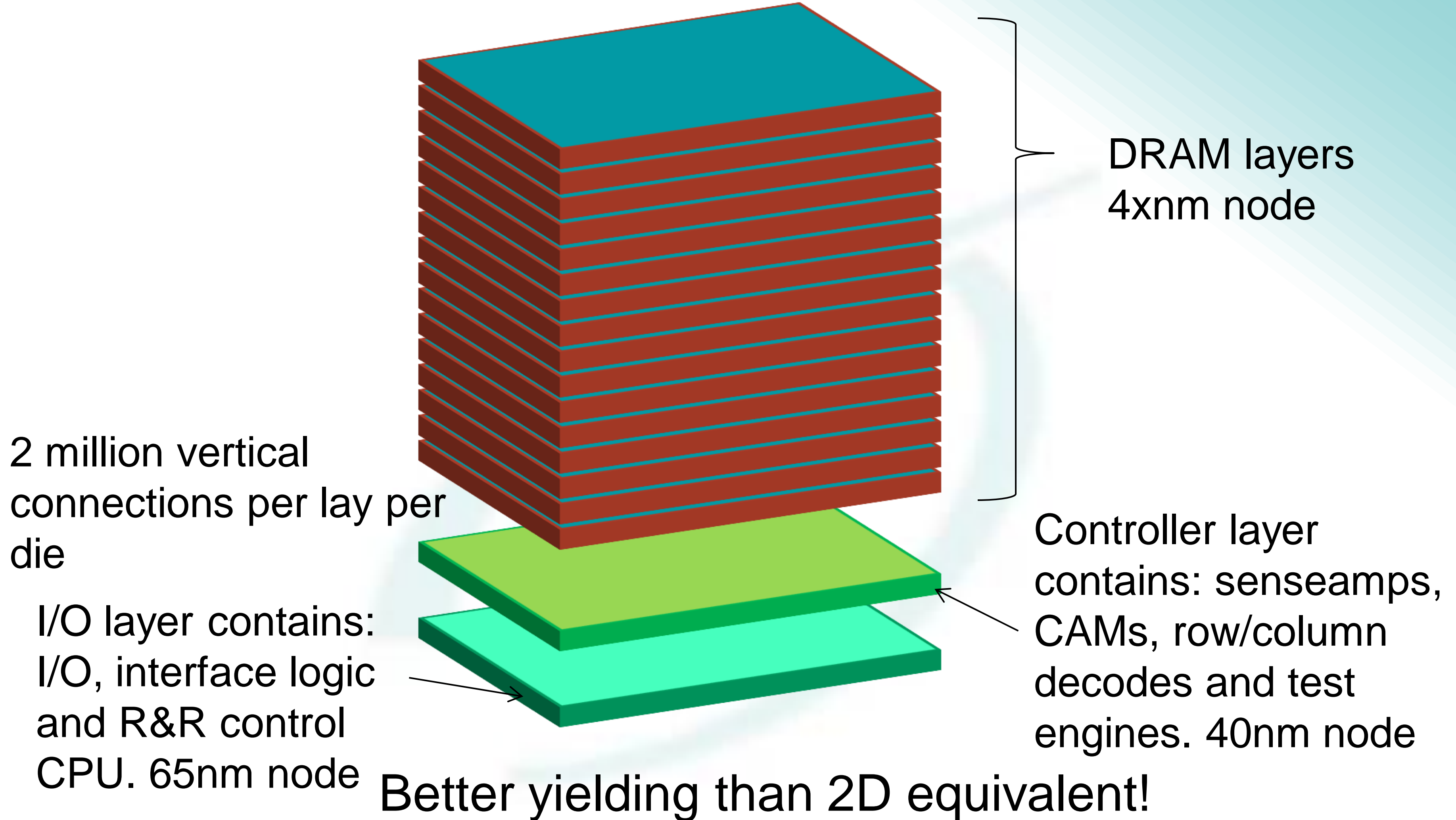


DiRAM4™

- 4-64Gb
- 64-256 Ports x 64bits (each way)
- @1GHz
  - 5-7ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >16Tb/s data transfer rate
  - 4096 banks
  - 2+2pJ/bit



DiRAM4 "Dis-Integrated" Memory



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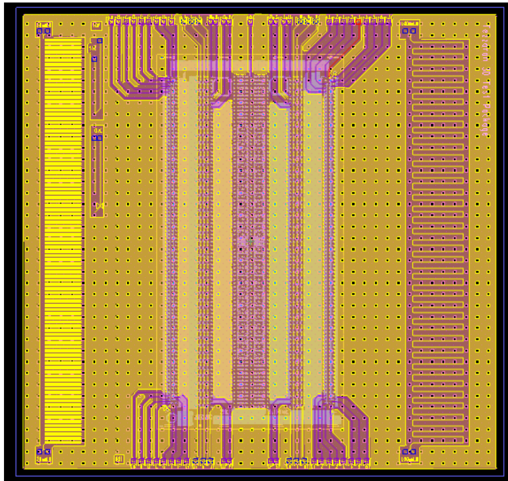
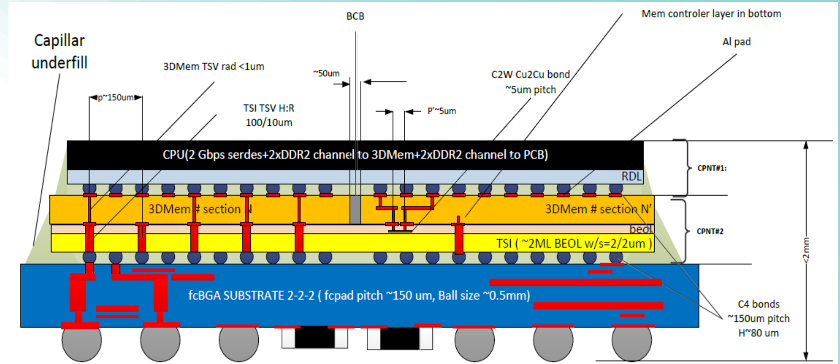
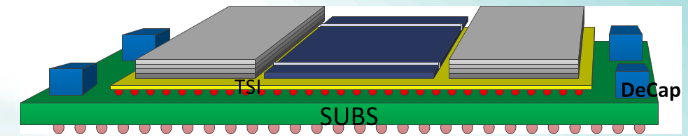
2.5/3D in Combination

IME A-Star /
Tezzaron
Collaboration





IME A-Star / Tezzaron
Collaboration



μBumps

Die to Wafer Cu Thermal Diffusion Bond

C4 Bumps

3 Layer 3D Memory

2 Layer Processor

FPGA (4Xnm)

C

level#4

level#3

Active Silicon Circuit Board

C

level#2

Organic Substrate

level#1

level#0

Solder Bumps

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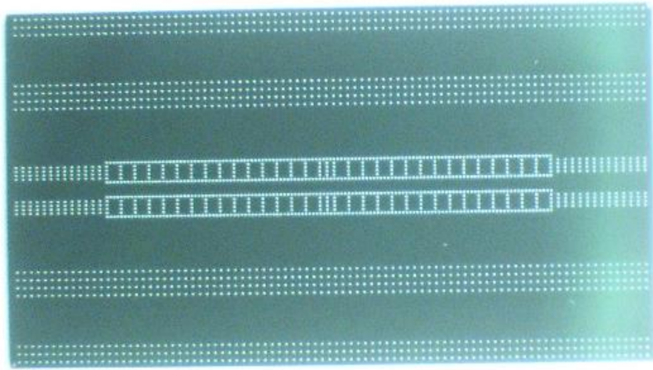
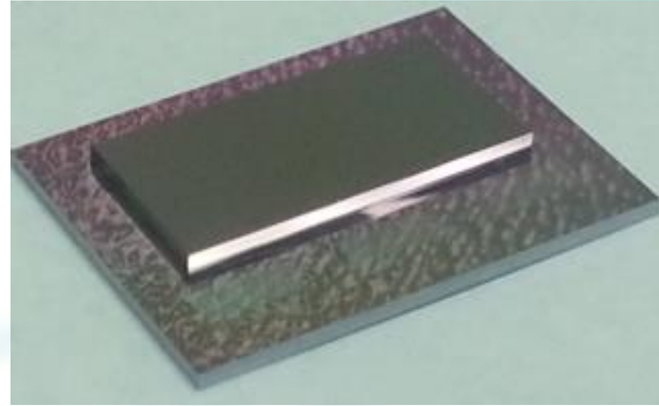
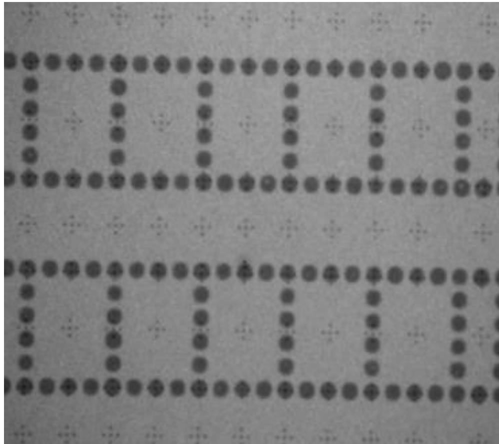
Tezzaron Dummy Chip C2C Assembly



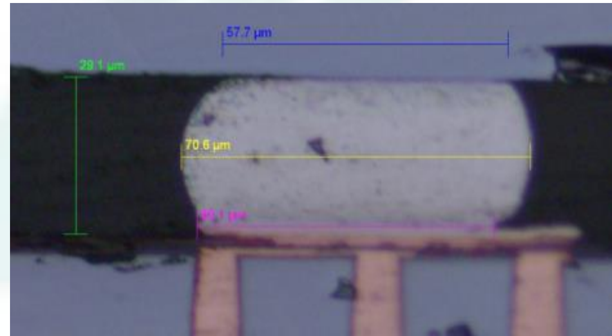
Memory die



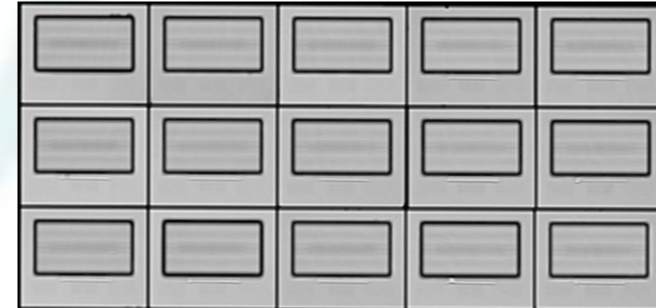
C2C sample



X-ray inspection indicated no significant solder voids



X-section of good micro bump



CSCAN showed no underfill voids (UF: Namics 8443-14)

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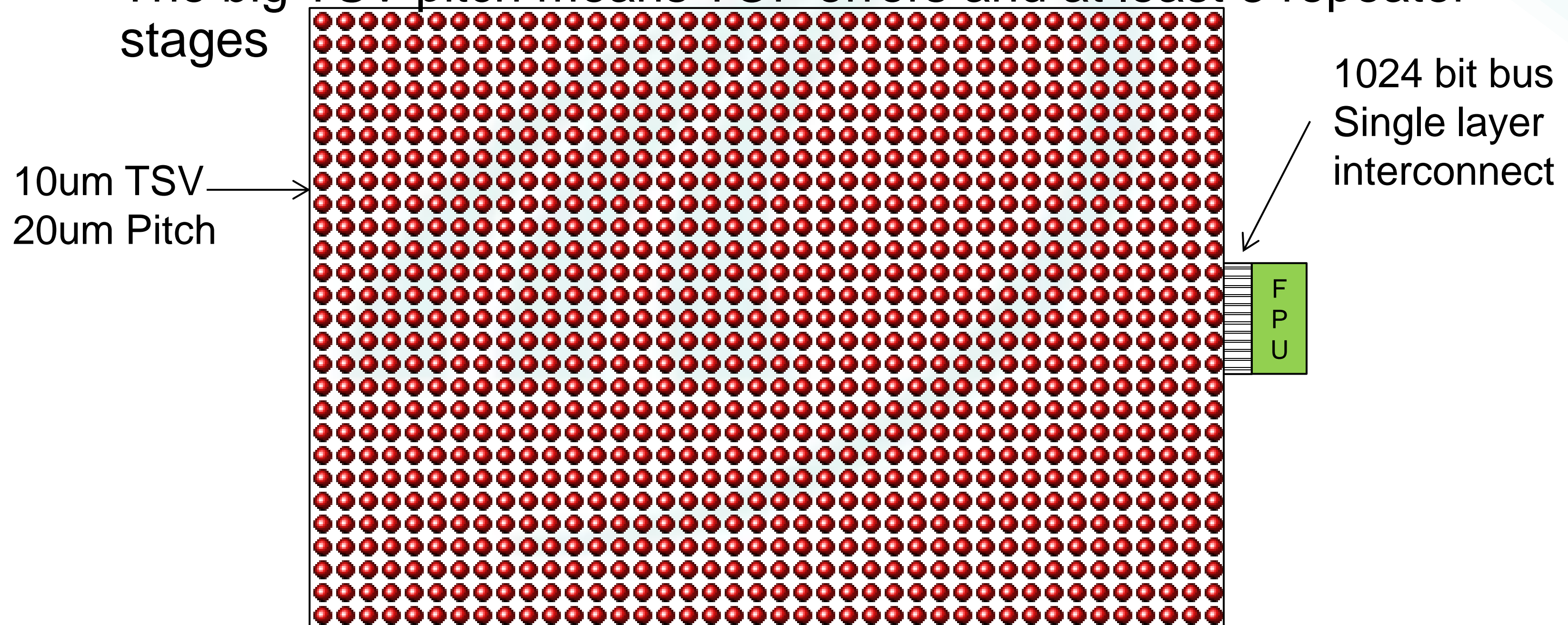
WHAT IS IMPORTANT?

TSV Pitch ≠ Area ÷ Number of TSVs

TSV pitch issue example

- 1024 bit busses require a lot of space with larger TSVs
- They connect to the heart and most dense area of processing elements
- The 45nm bus pitch is ~100nm; TSV pitch is >100x greater
- The big TSV pitch means TOF errors and at least 3 repeater stages



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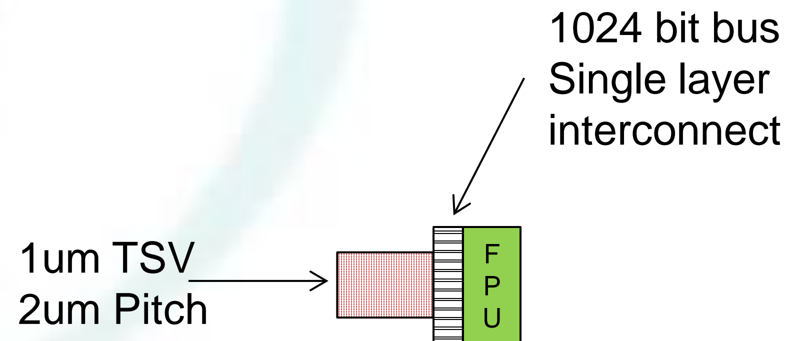

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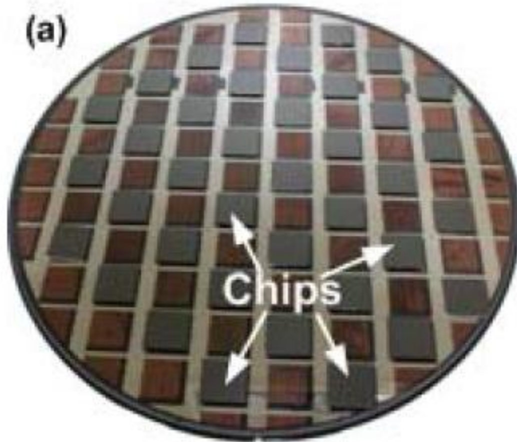
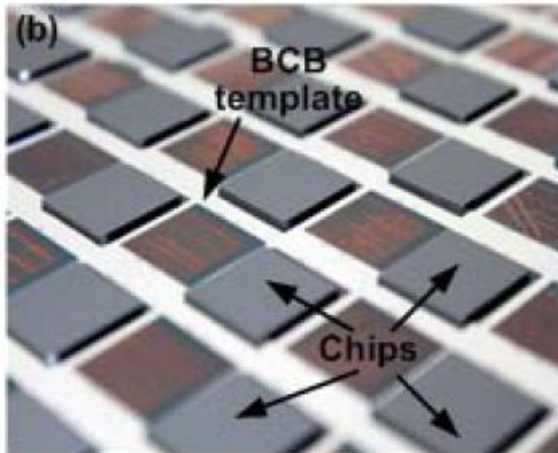
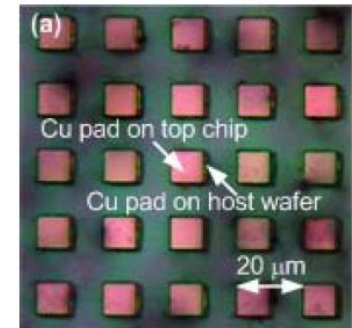
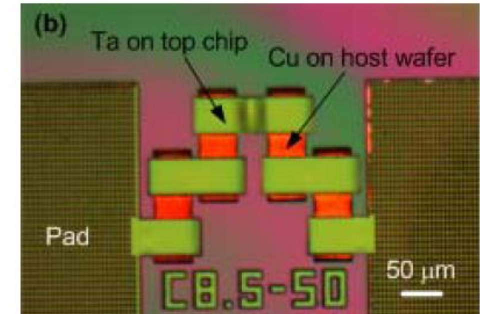
Die to Wafer – 2.5D







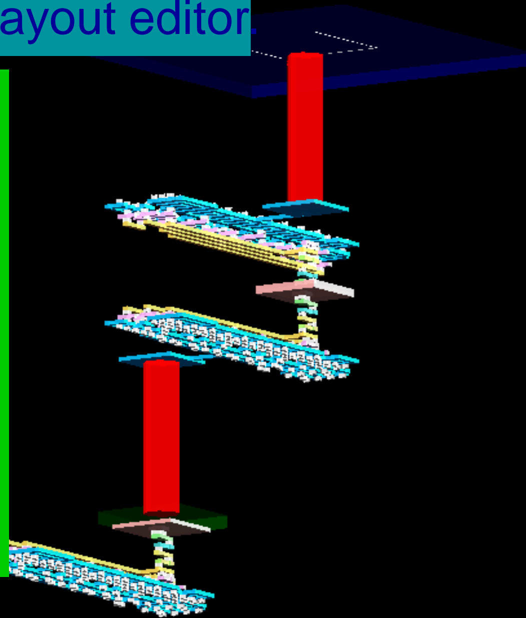
RPI/Dr. James Lu



- KGD
- Multilayer capability
- Incremental risk buy down
- Extends SOC concepts

Tools

MAX-3D by Micro Magic, Inc.
Fully functional 3D layout editor.



- Independent tech files for each tier.
- Saves GDSII as flipped or rotated.
- Custom output streams for 3D DRC / LVS.

DRC, LVS, Transistor synthesis, Crossprobing.
Multiple tapeouts, 0.35um-45nm
>20GB, ~10B devices

Mentor Graphics®

Mentor and Tezzaron Optimize Calibre 3DSTACK for 2.5/3D-ICs

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What Has Tezzaron Learned?

- Systems require multiple solutions
  - SIP is the future of SOC
  - Logic, Memory, Analog, MEMS, Photonics, Cooling
    - InP, GaAs, SiGe, GaN, CNT
- To practice 2.5 and 3D you need multiple technologies
  - Cu-Cu
  - DBI
    - 150C bonding
  - Oxide, IM, gold
  - Via middle
  - Via last
  - Cu TSV
  - W TSV

Tezzaron/Novati

- “Volume” 2.5D and 3D Manufacturing in 2013
- Interposers
- Future interposers with
  - High K Caps
  - Photonics
  - Passives
  - Power transistors
- Wholly owned Tezzaron subsidiary
- Cu-Cu, DBI®, Oxide, IM 3D assembly

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NOVATI TECHNOLOGIES, INC.

Facility Overview

Capabilities

- Over 150 production grade tools
- 68000 sq ft Class 10 clean room
- 24/7 operations & maintenance
- Manufacturing Execution Systems (MES)
- IP secure environments, robust quality systems
- ITAR registered
- Full-flow 200mm silicon processing, 300mm back-end (Copper/Low-k)
- Process library with > 25000 recipes
- Novel materials (ALD, PZT, III-V, CNT, etc)
- Copper & Aluminum BEOL
- Contact through 193nm lithography
- Silicon, SOI and Transparent MEMS substrates
- Electrical Characterization and Bench Test Lab
- Onsite analytical tools and labs: SIMS, SEM, TEM, Auger, VPD, ICP-MS, etc

- ISO 9001:2008 13485:2013
- TRUST 2013

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The Big Problems Left Are…

- Test
  - 5k I/O going to 20k I/O going to 100k I/O
  - When is the testing good enough?
    - Biggest hidden cost
- The right processes
  - HVM scaling
- The heavy CAD tools
  - 3D aware synthesis, P&R
    - We don’t know what we don’t know

Ongoing: Work to be Done

New Data Needs and Standards

- Notch
- Orientation limitations
- Run out / street size / magnification
- Die location
- TCE matching / stress / warpage
  - TCE zero match at what temperature?
- Materials
- Planarity
- Surface roughness

Decisions to Make

2.5D Alternatives

- Silicon Interposers
  - 2-3um L/S/D
  - Rs and Cs
  - Active is the future
  - Handling & handoff
- Organics
  - 5-6 um
    - Litho limits
    - Material planarity limits
  - Great cost structure
  - TCE Challenges
  - Large substrate
- Glass
  - Large substrate

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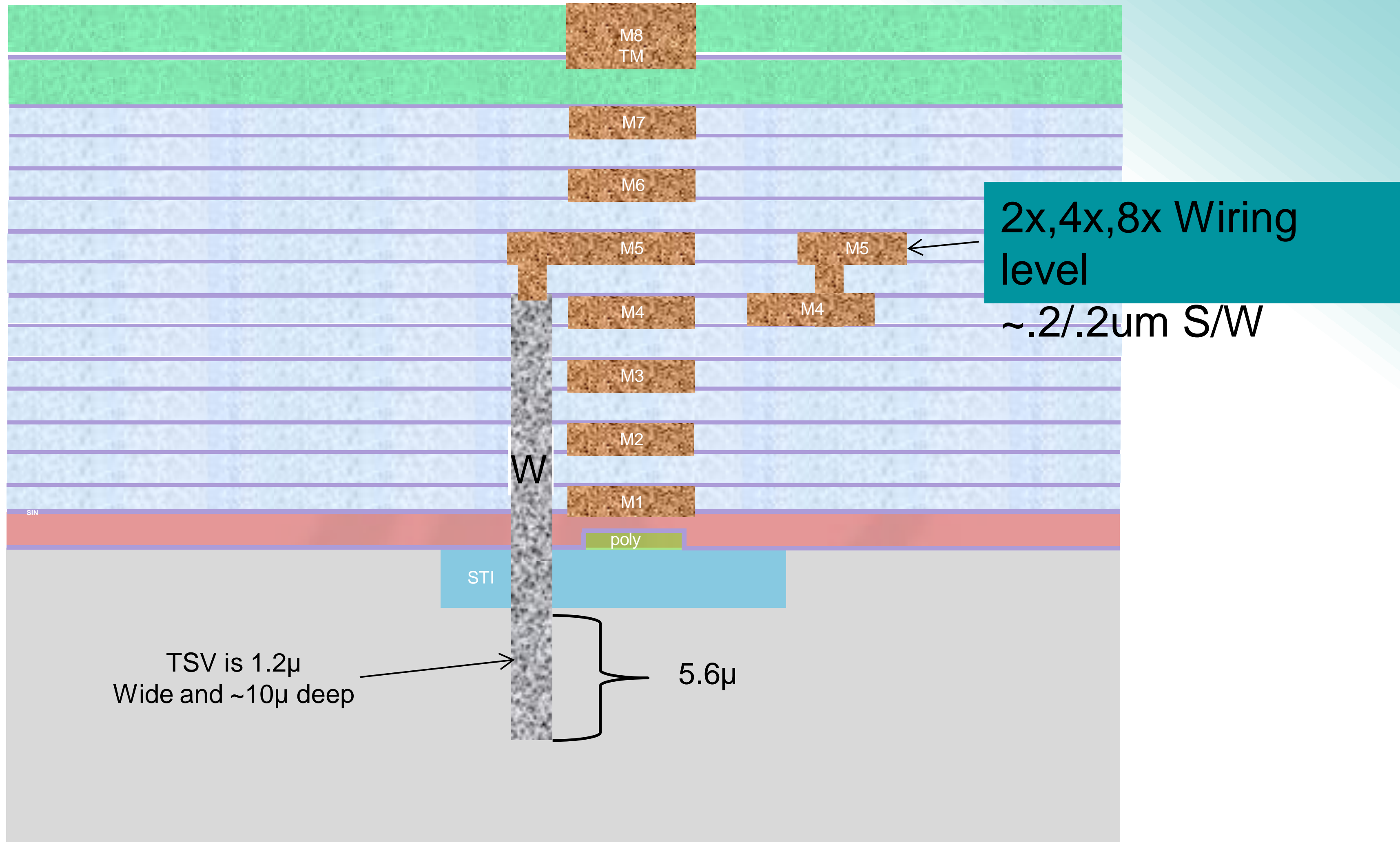
THE ROAD AHEAD…

Near End-of-Line TSV Insertion



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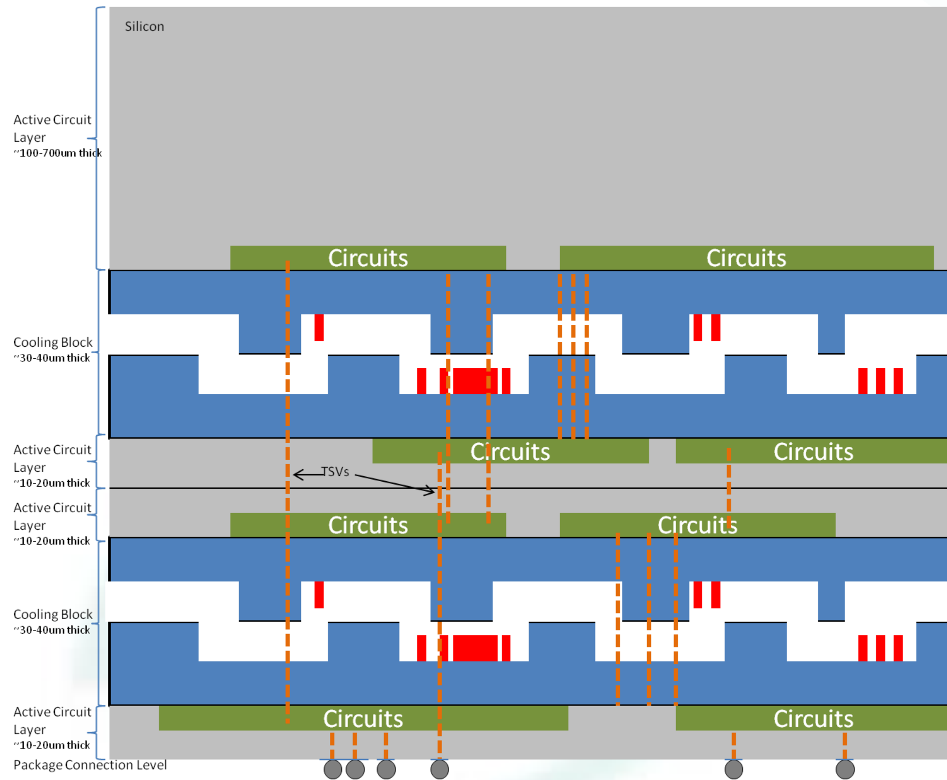
Photonics for Short Haul

14nm FF Chip

- 16x100G Optical Transceivers
  - 8 Optical I/O per Couplers
- Four optical power supplies

- Photonic Interposer with TSVs

Integrating Fluidics into 3D: Liquid Cooling



It's a MEMS, 2.5D SOC/SIP future…

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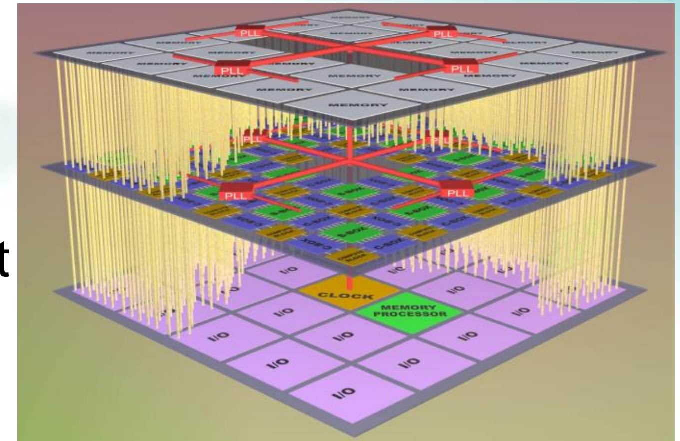
“5.5D” Systems

- SIP/SSIP
  - Power Conversion
  - Cooling
  - Photonics
- Optimization
  - Extending to power
- Mixed PCB/IC Metaphor

Summary

- Industry has the momentum
  - Generating tools and technology
  - Problems are now deemed solvable
- 3D is proving value
  - There is production and it is expanding
- Lingering questions about who does what
  - Foundry to OST interface
- Test and HVM processes are the growth opportunities



Sensors

Computing

MEMS

Communications

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