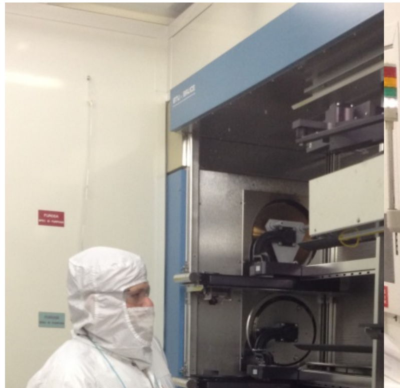
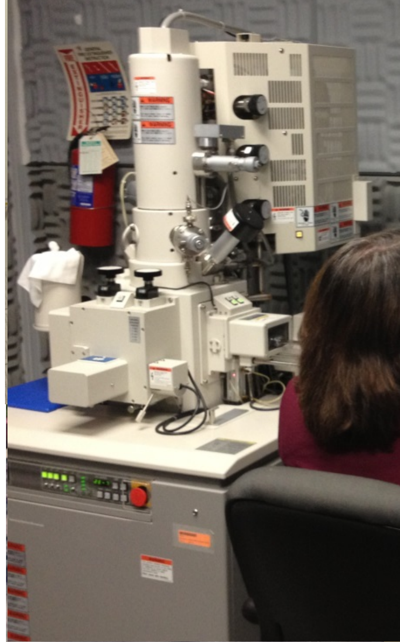
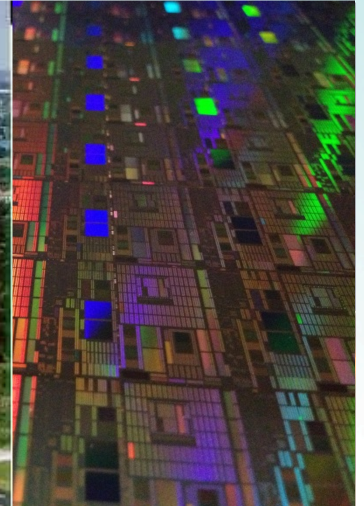
The 3rd Wave: Hyper Performance and the End of Commodity Memory

David Chapman
VP Marketing

An Introduction…







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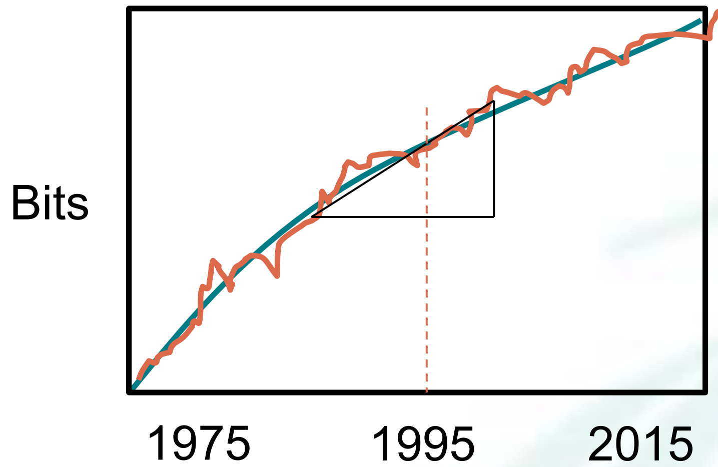
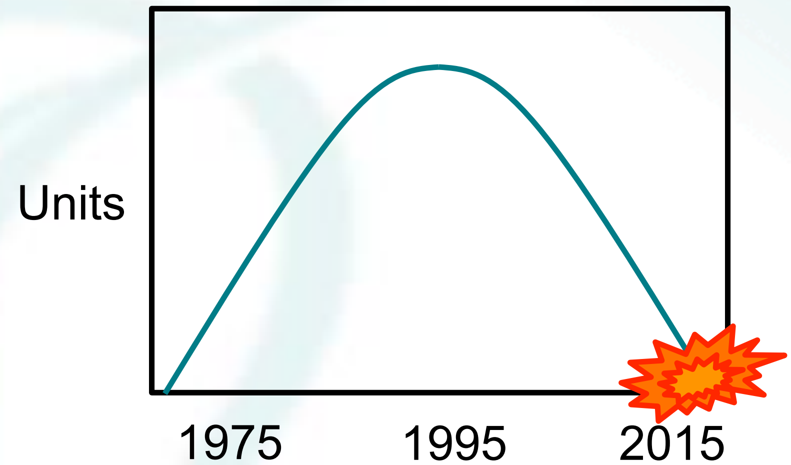
SEMICONDUCTOR

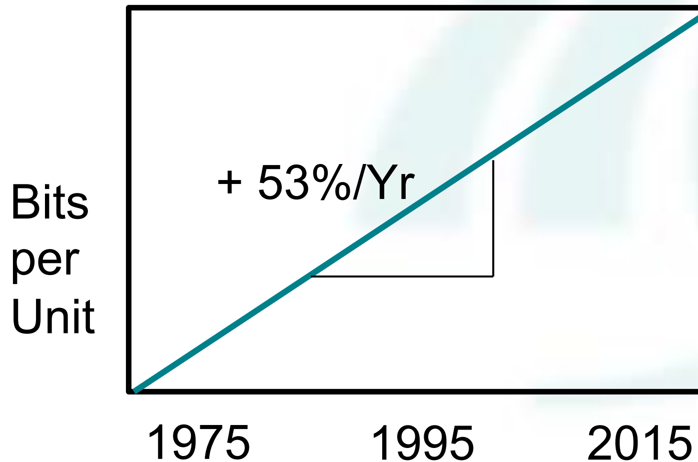
Feeling Warm?

http://hairpinturnsahead.typepad.com/.a/6a0133ec7b075a970b01bb07aa594c970d-pi

The First 40 Years of DRAM







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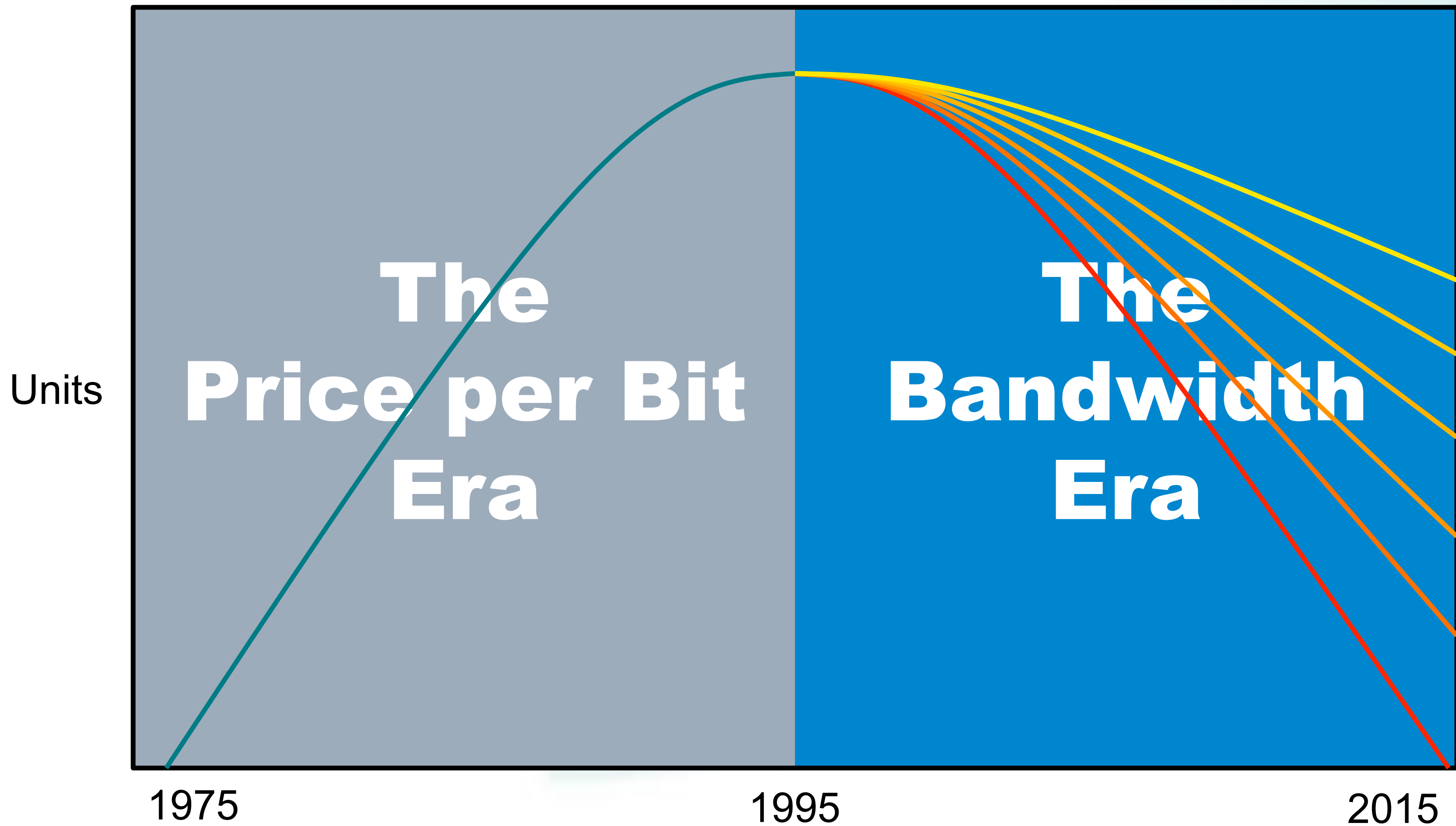
The First Transformation



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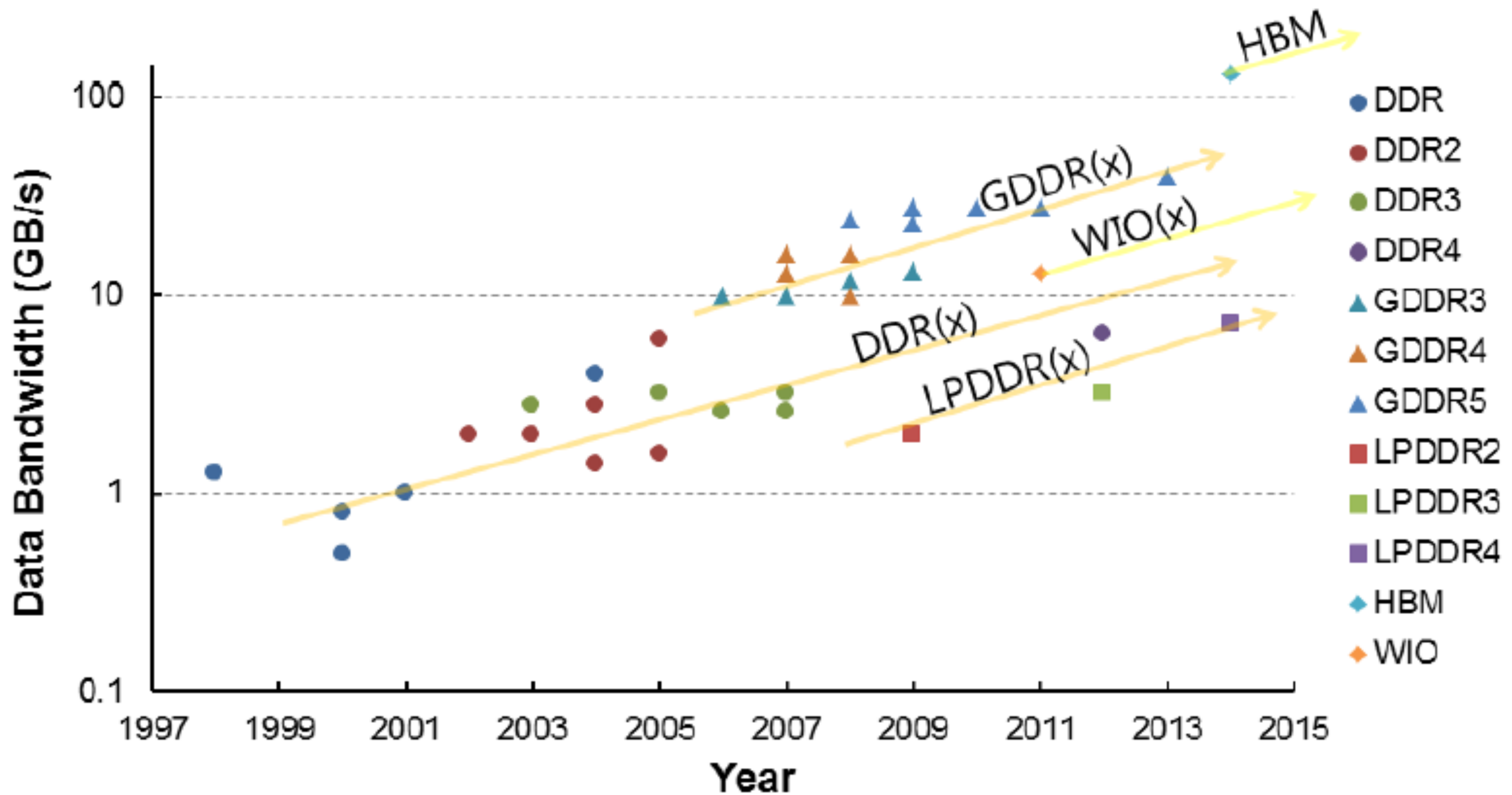
DRAM Data Bandwidth



http://tech4gizmos.com/70/

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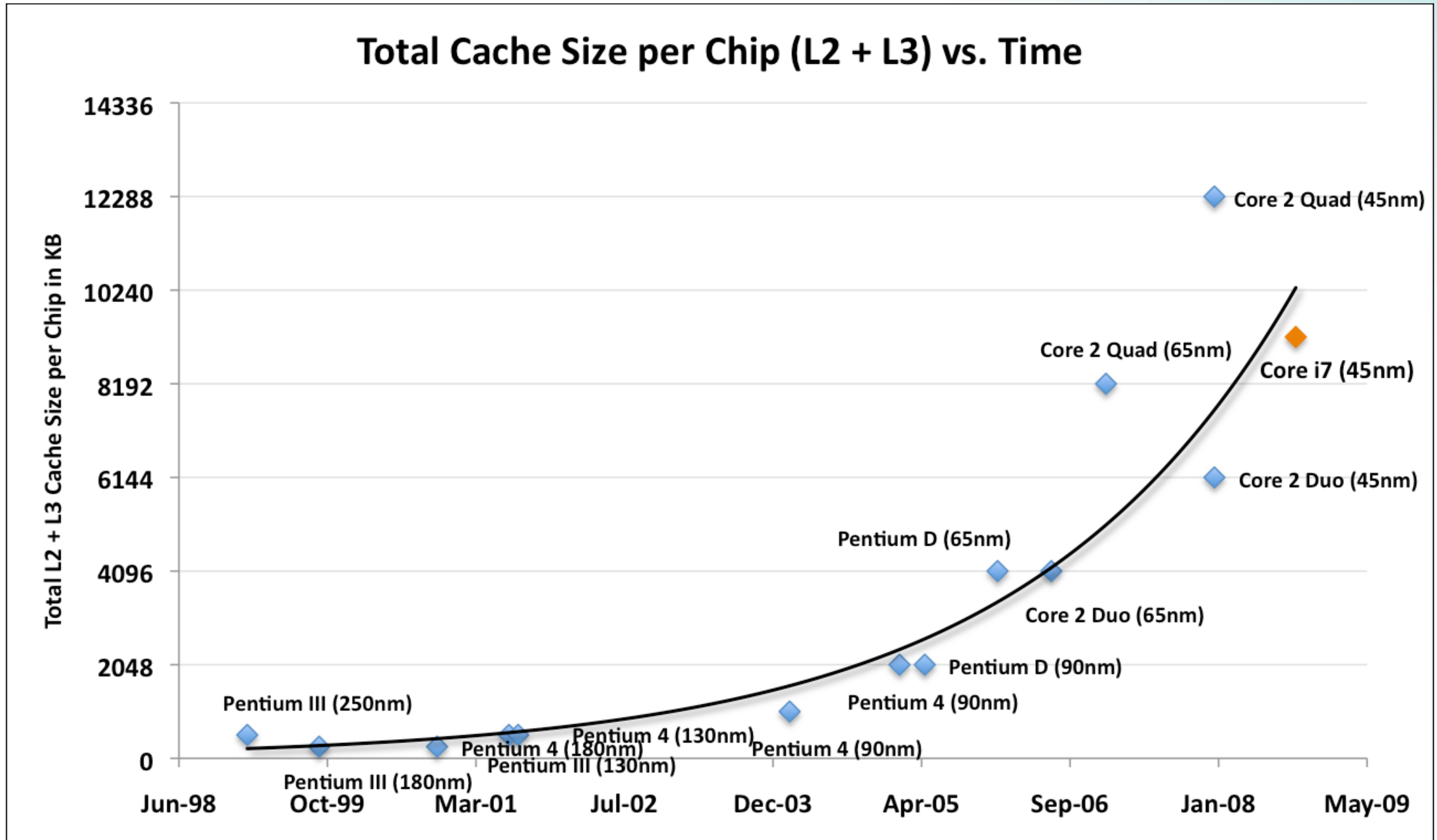
Cache Gone Wild



http://images.anandtech.com/reviews/cpu/intel/nehalem/part3/totalcache.png

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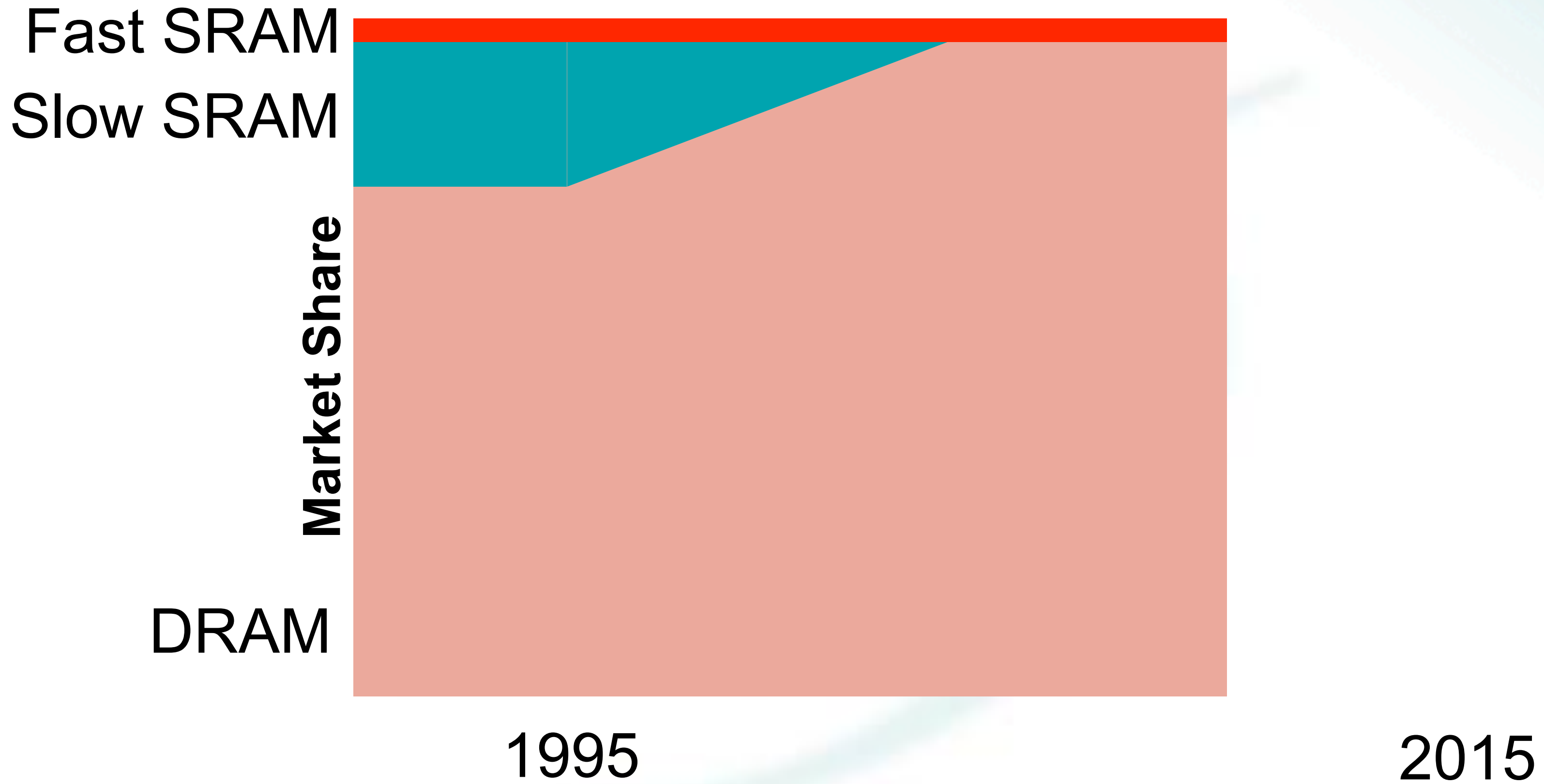
The Long Boil



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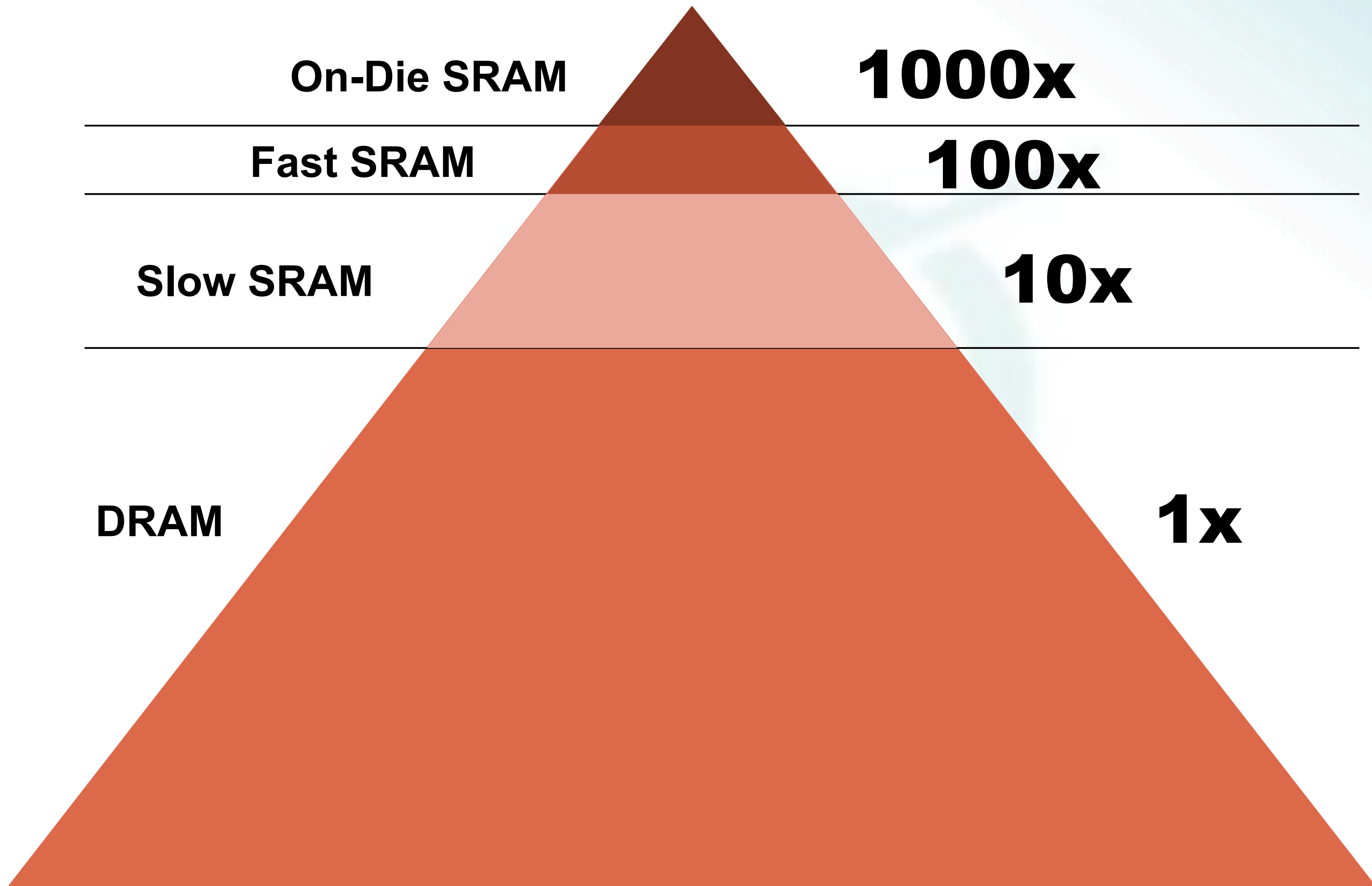
Volatile RAM Hierarchy



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DRAM Vendor Base

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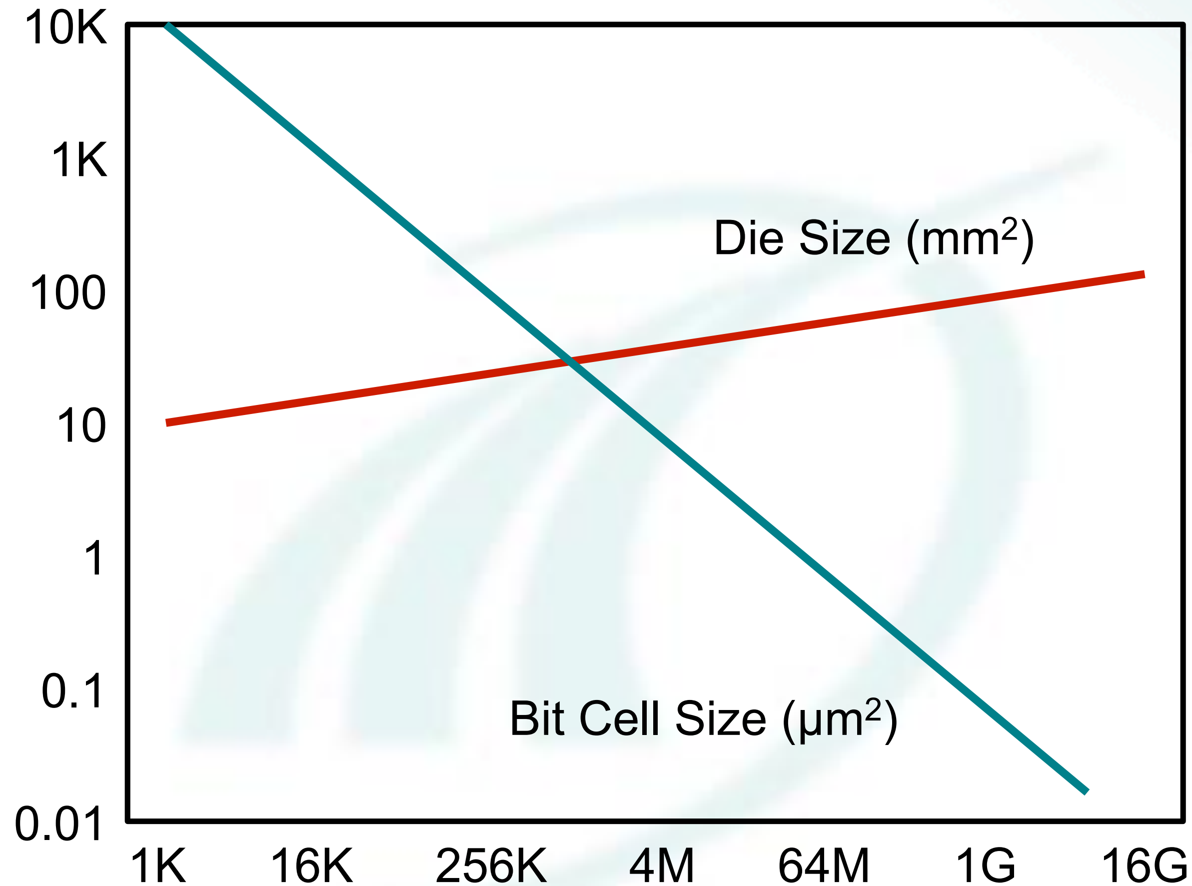
Bits Shrink – Die Grow



http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/dimension-increase-in-metal-oxide-semiconductor-memories-and-transistors

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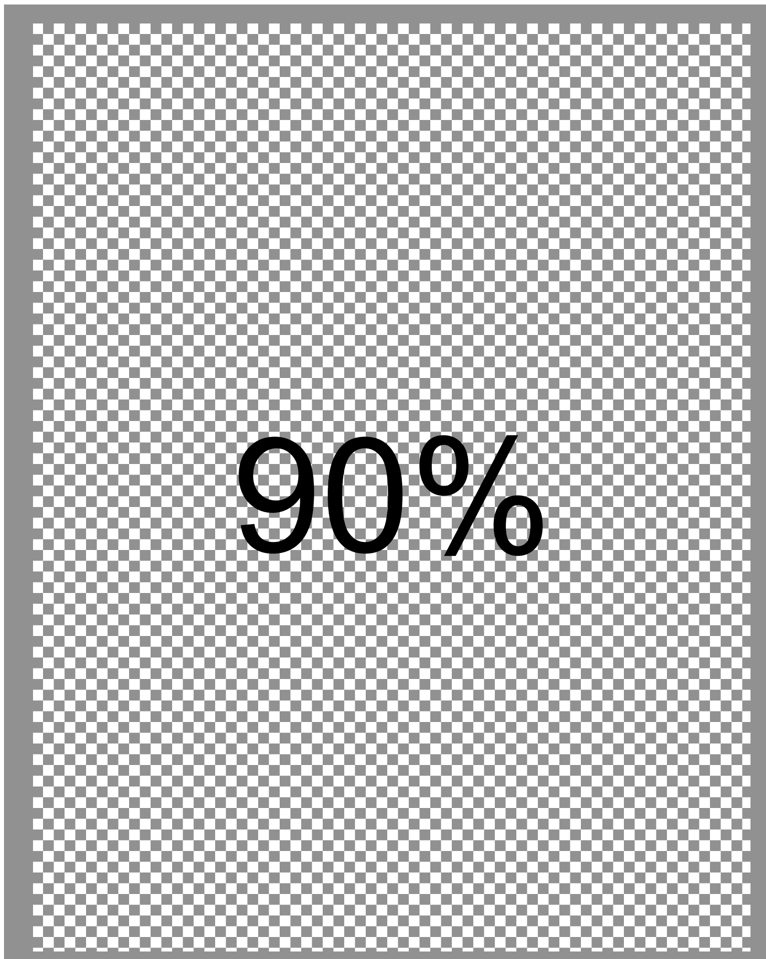
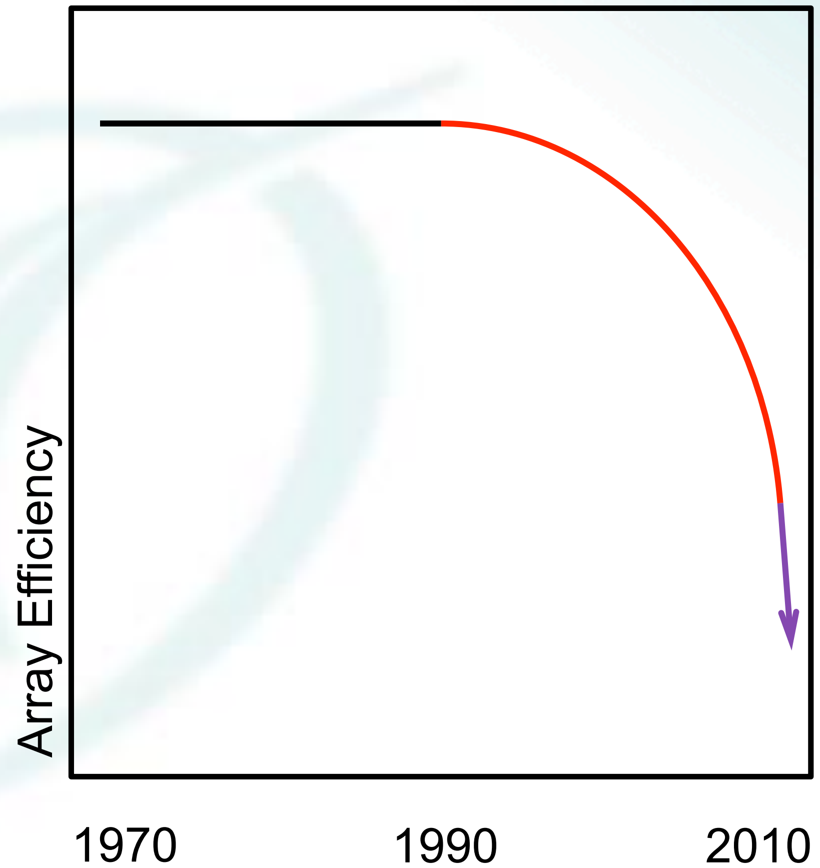
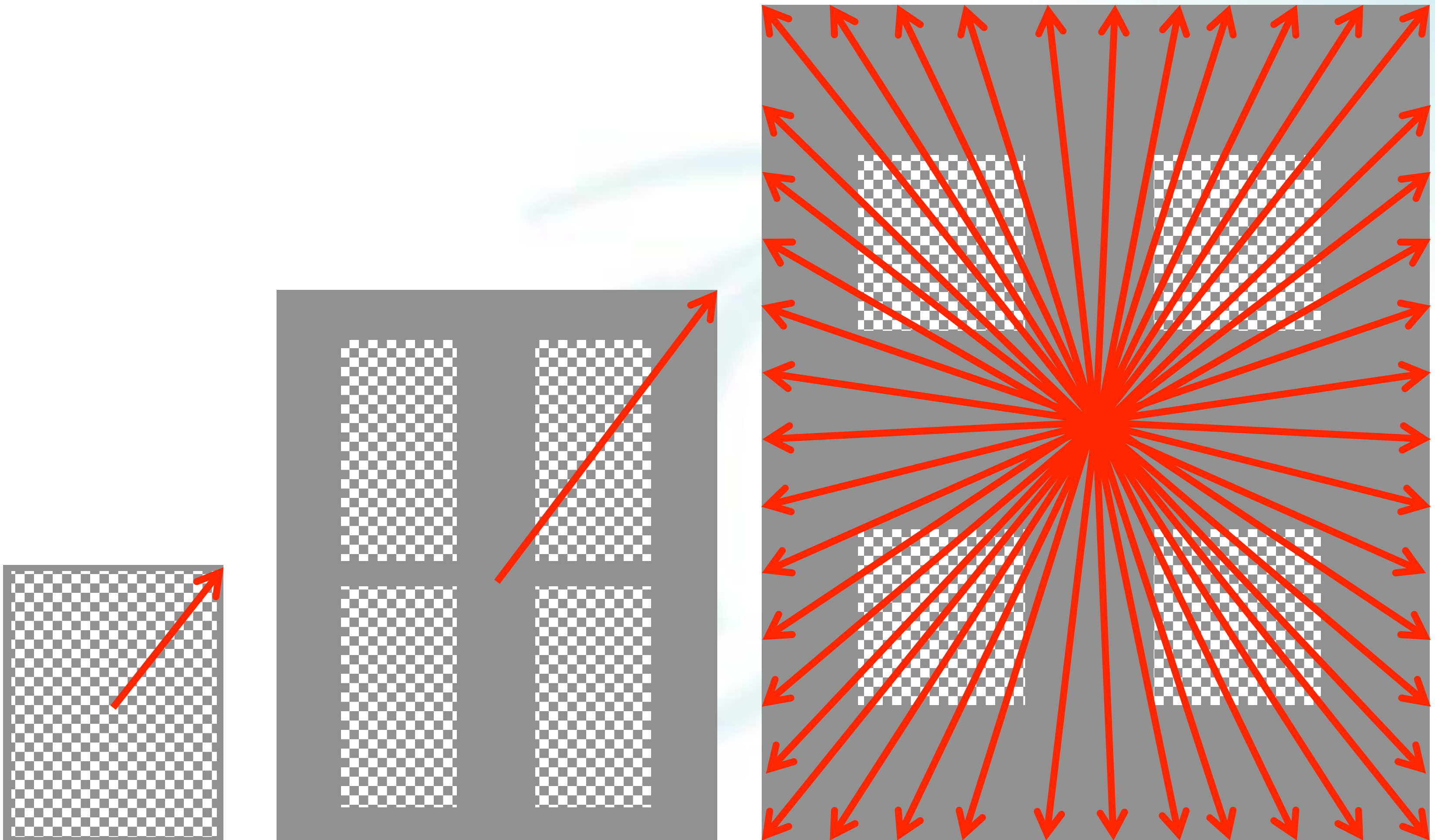
Array Efficiency





On-Die Routing Dominates



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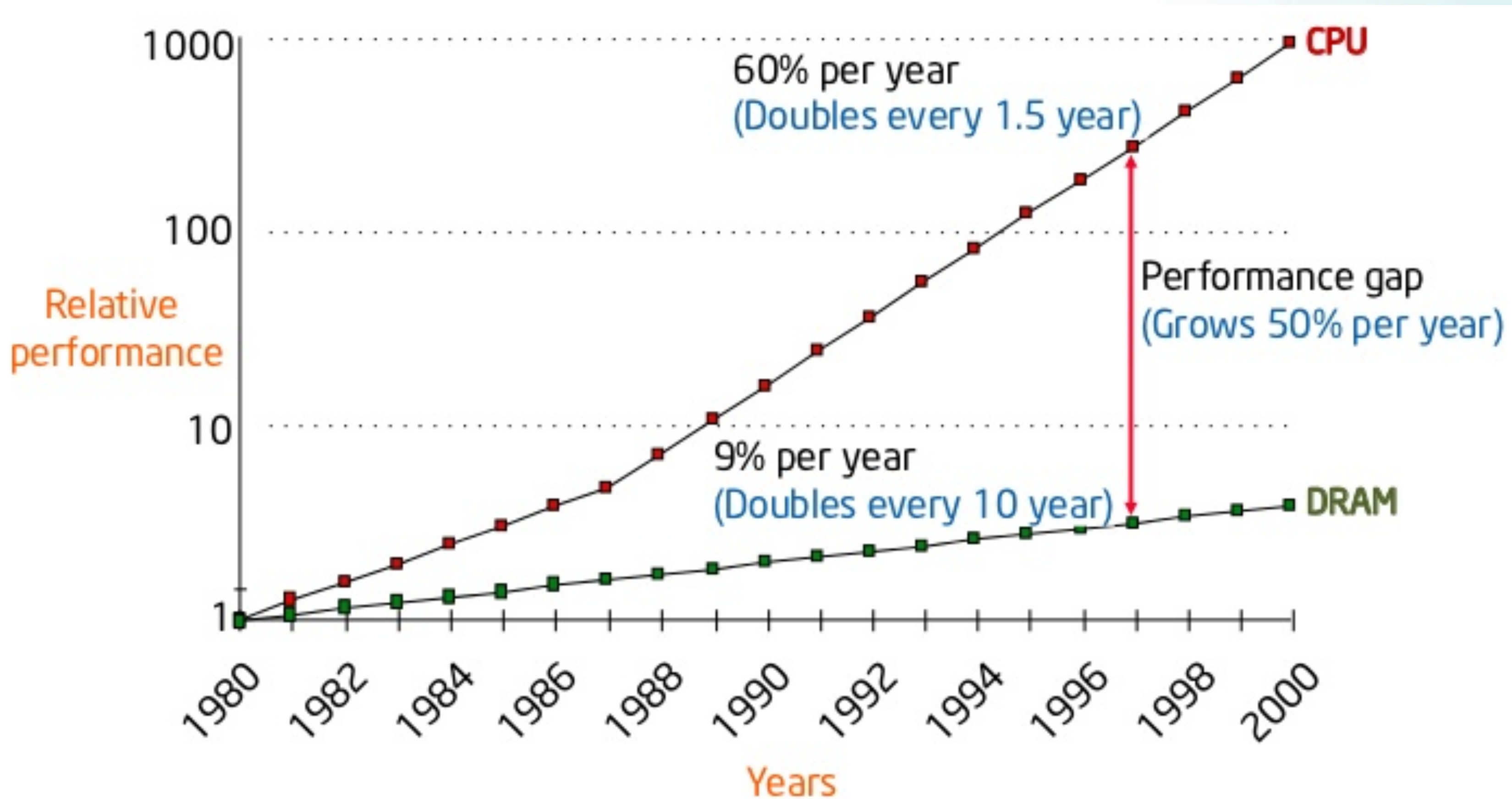
The Gap



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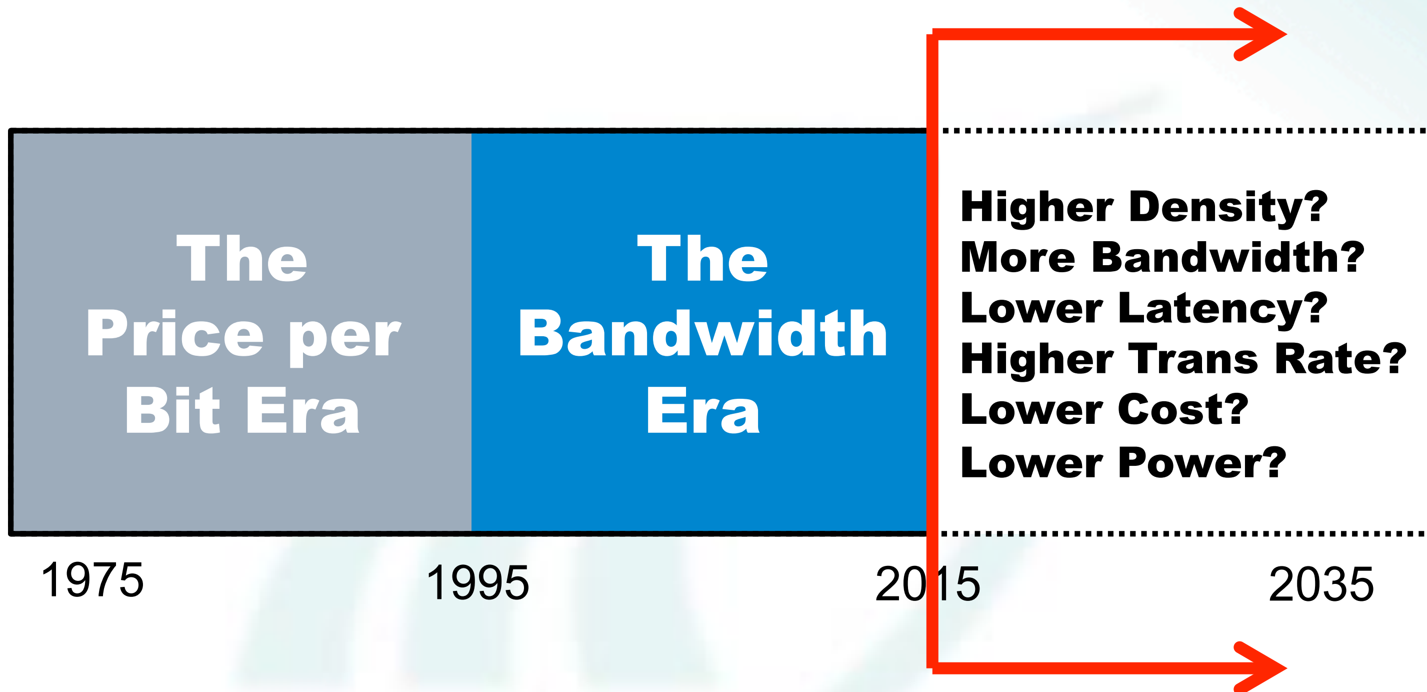
Not Dead Yet

http://megaodd.com/wp-content/uploads/2015/01/70ae5__FoodsEatenAlive07-650x401.jpg

The Next 20 Years



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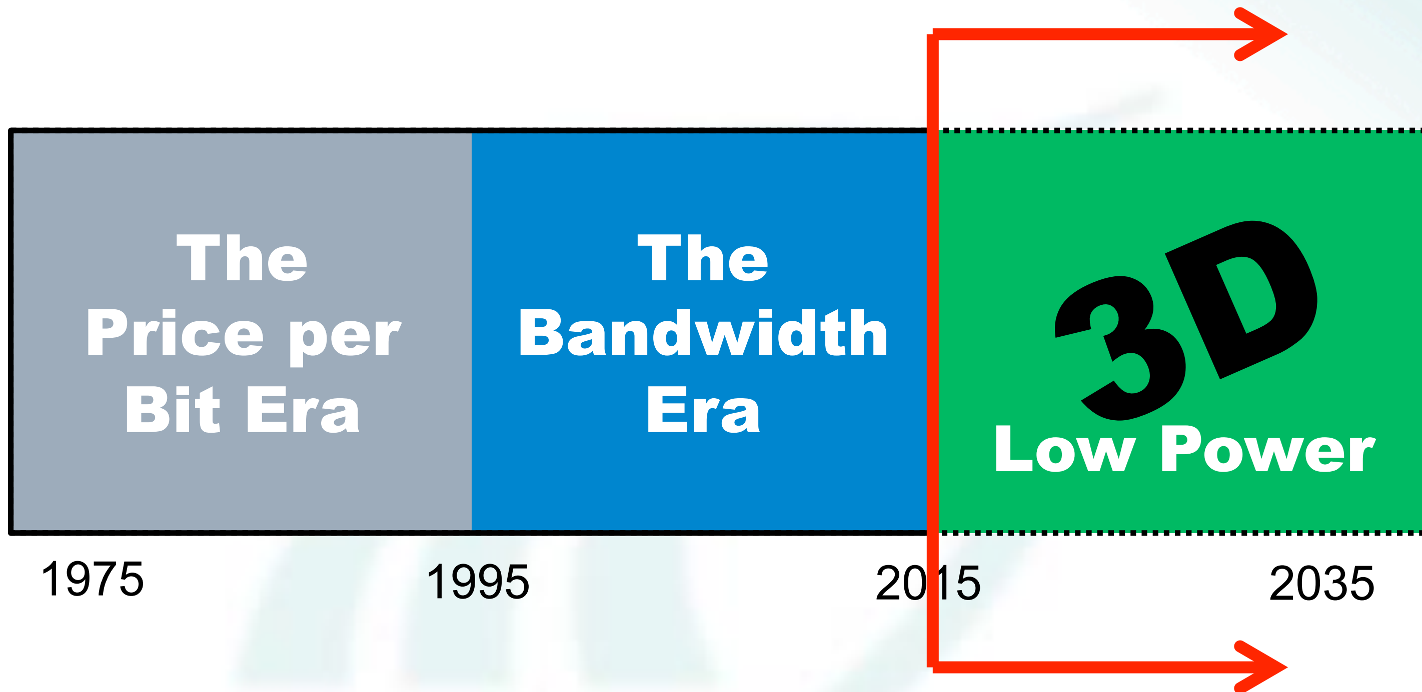
Bandwidth is NOT the Problem

"The problem isn't memory bandwidth — it's memory latency and memory power consumption."

Forget Moore's law: Hot and slow DRAM is a major roadblock to exascale and beyond
By Joel Hruska on July 14, 2014 @ http://www.extremetech.com

http://www.extremetech.com/computing/185797-forget-moores-law-hot-and-slow-dram-is-a-major-roadblock-to-exascale-and-beyond

The Next 20 Years



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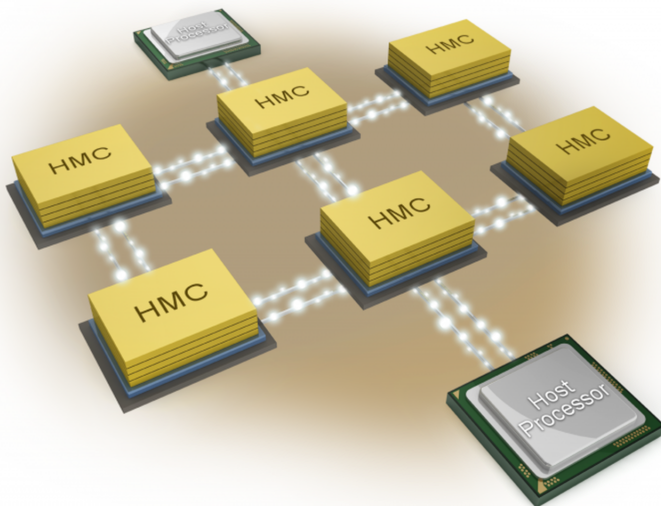
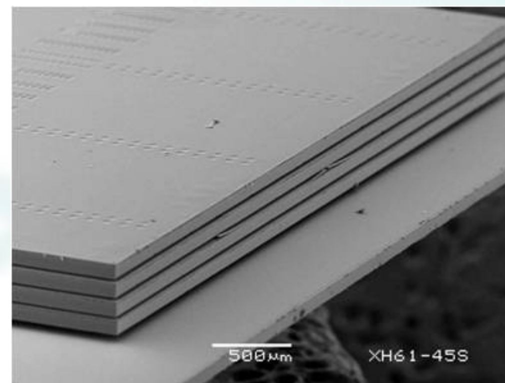
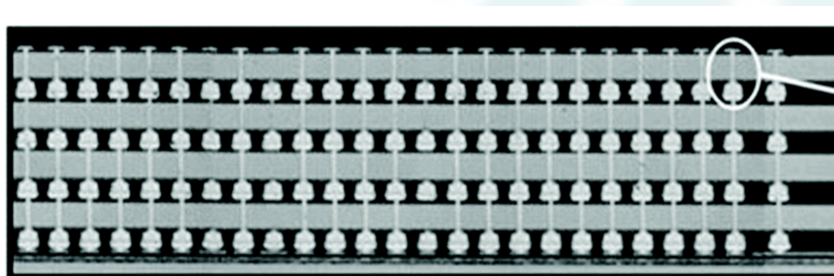
Micron HMC



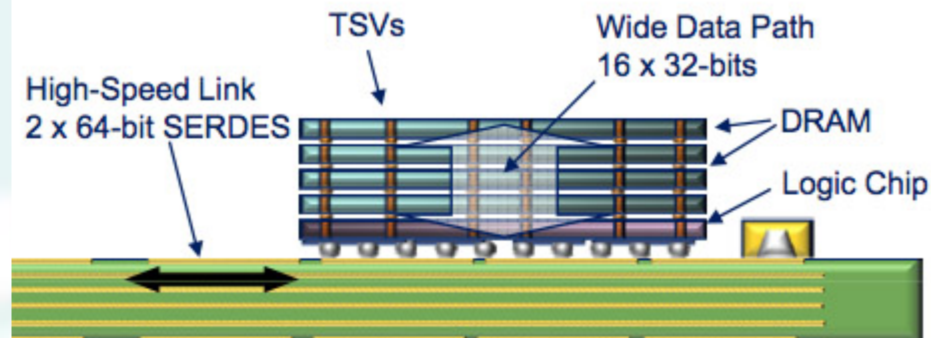
http://www.extremetech.com/computing/167368-hybrid-memory-cube-160gbsec-ram-starts-shipping-is-this-the-technology-that-finally-kills-ddr-ram



http://www.anandtech.com/show/4819/intel-and-micron-develop-hybrid-memory-cube-stacked-dram-is-coming



http://wiley-vch.e-bookshelf.de/products/reading-epub/product-id/2418826/title/handbook+of+3d+integration.html?lang=en



https://www.semiwiki.com/forum/content/1610-3d-memories.html

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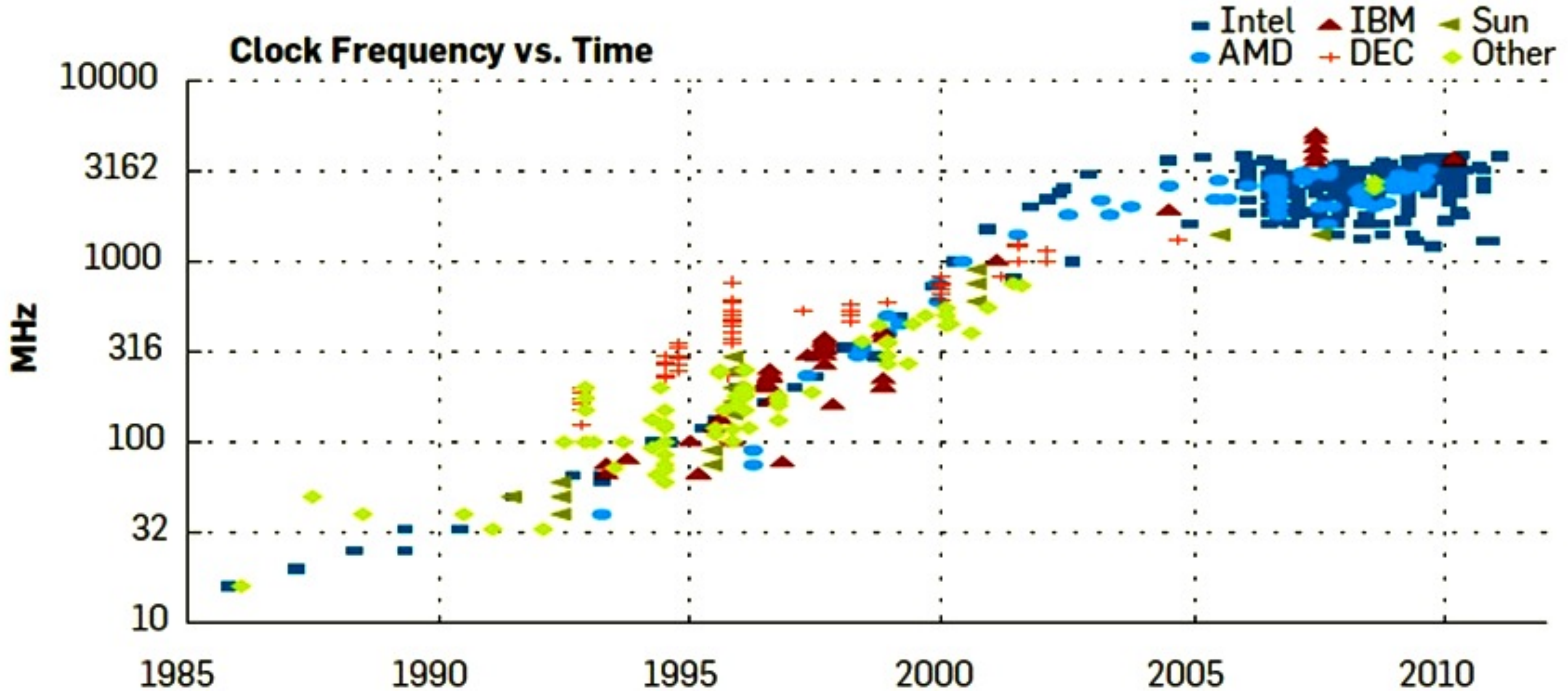
Clocking Stalls



http://deliveryimages.acm.org/10.1145/2140000/2133822/figs/f7.jpg

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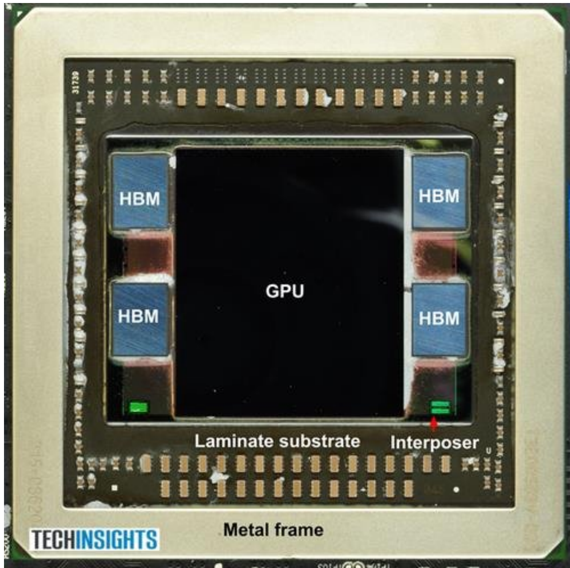
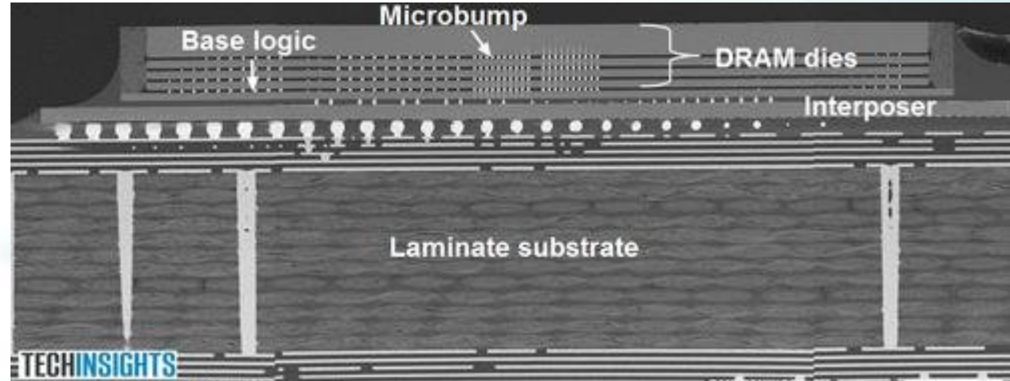
Hynix HBM





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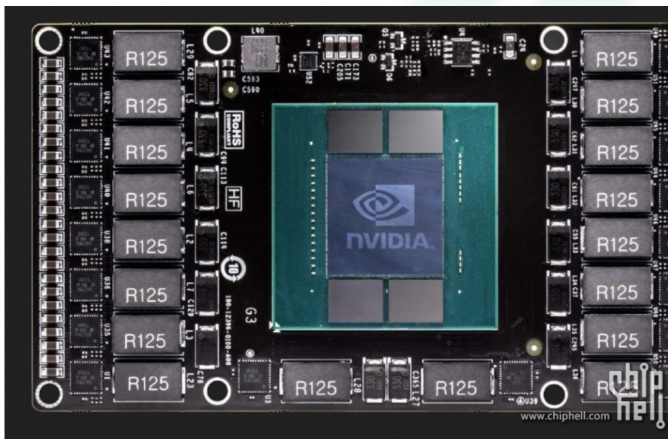

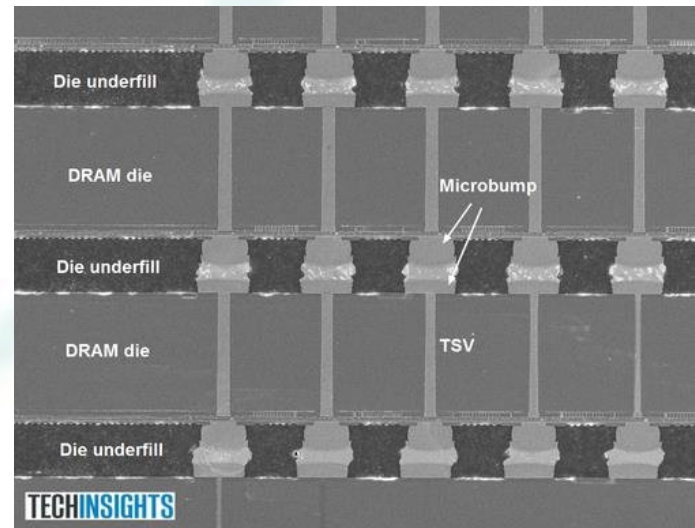

http://wccftech.com/nvidia-pascal-gpu-17-billion-transistors-32-gb-hbm2-vram-arrives-in-2016/

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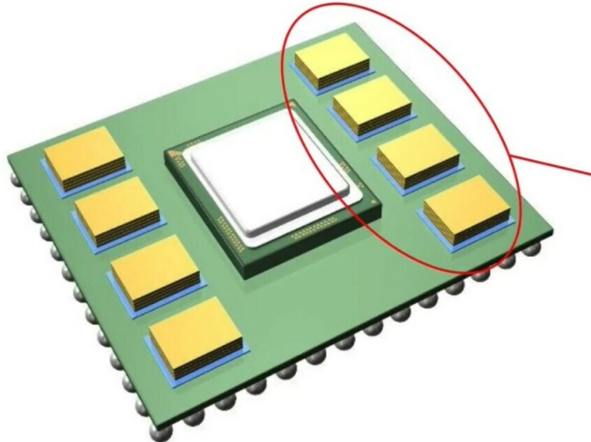
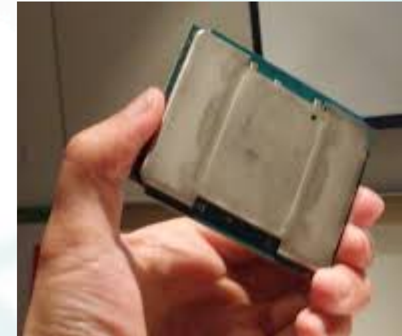
http://www.pcper.com/news/General-Tech/Learn-bit-more-about-Knights-Landing

Intel *Knight's Landing* HPC Processor

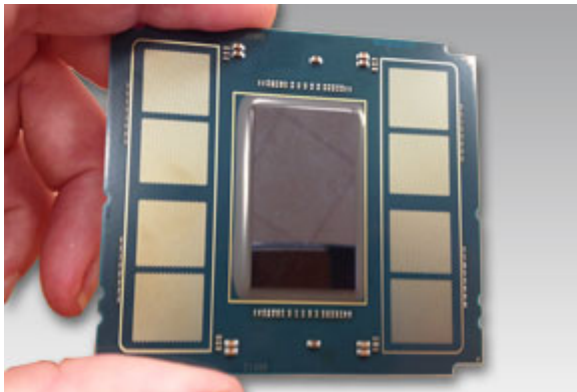


- 5X the bandwidth v. GDDR5
- Up to 16GB
- One-third the footprint
- Half the energy per bit
- Managed memory stack for optimal levels of reliability, availability and serviceability



http://news.cecb2b.com/info/20150326/3082445.shtml

http://electroiq.com/insights-from-leading-edge/2014/06/iftle-198-intel-to-commercialize-micron-hmc-3d-stacked-memory-in-hpc-processor-gs-nanotech-announces-3dic-plans-statschippac-suitors-named/



3+ TFLOPS[1]
In One Package
Parallel Performance & Density

New for Knights Landing
(Next Generation Intel® Xeon Phi™ Products)

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors

Compute: Intel® Silvermont Arch. (Intel® Atom™)[2]
- Low-Power Cores with HPC Enhancements[3]
- 3X Single Thread Performance[4] vs Prior Gen.
- Intel Xeon Processor Binary Compatible[5]

Intel® Silvermont Arch. Enhanced for HPC[6]
Integrated Fabric
Processor Package

On-Package Memory: High Performance
- up to 16GB at launch
- 1/3X the Space[6]
- 5X Bandwidth vs DDR4[7]
- 5X Power Efficiency[6]

Jointly Developed with Micron Technology

http://www.eweek.com/servers/us-blocks-intel-from-supplying-chips-for-chinese-supercomputers.html

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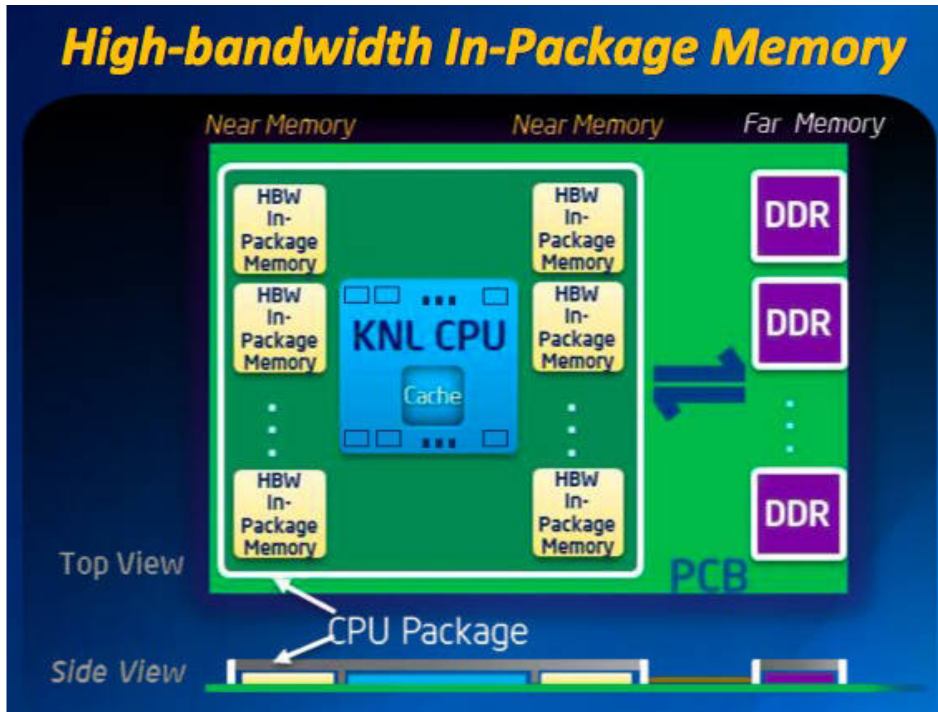
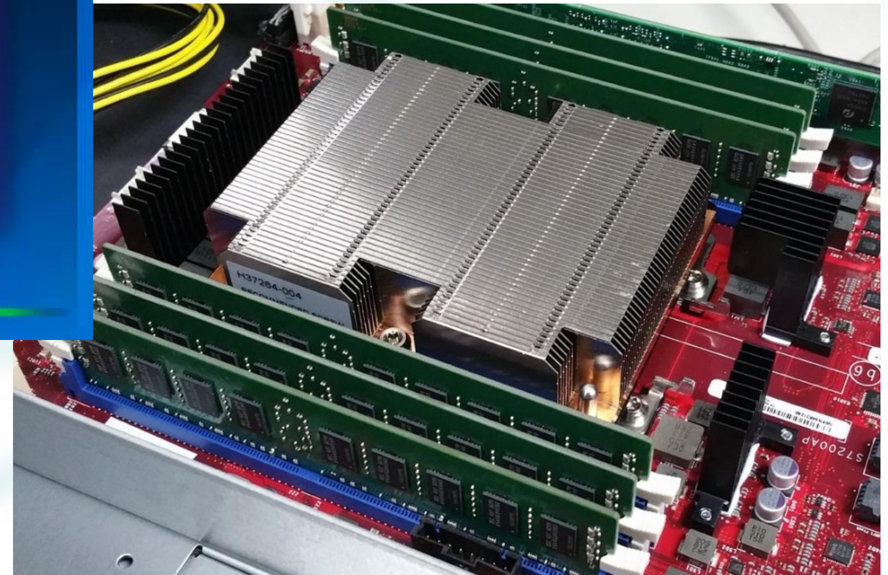
High Performance "Near" Memory



http://forums.anandtech.com/showthread.php?t=2388600



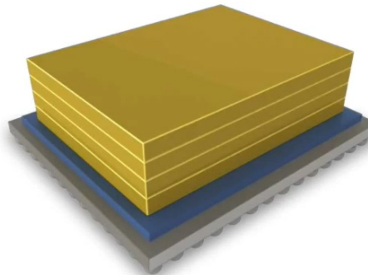
http://cdn.wccftech.com/wp-content/uploads/2015/03/Intel-Knights-Landing-Processor_Adams-Rack.jpg

Bandwidth?

Introducing MCDRAM

MCDRAM (multi channel DRAM)

The innovative in-package memory found in Intel's next-generation Xeon Phi co-processor, MCDRAM (multi channel DRAM) is a customized memory interface that leverages the two company's ongoing collaboration and promises to deliver the performance and efficiency gains required by next generation HPC systems.



Micron's High Performance Stacked Memory Solution

6 June 16, 2014 | ©2014 Micron Technology, Inc.

Micron

http://images.anandtech.com/doci/8217/MCDRAM.jpg

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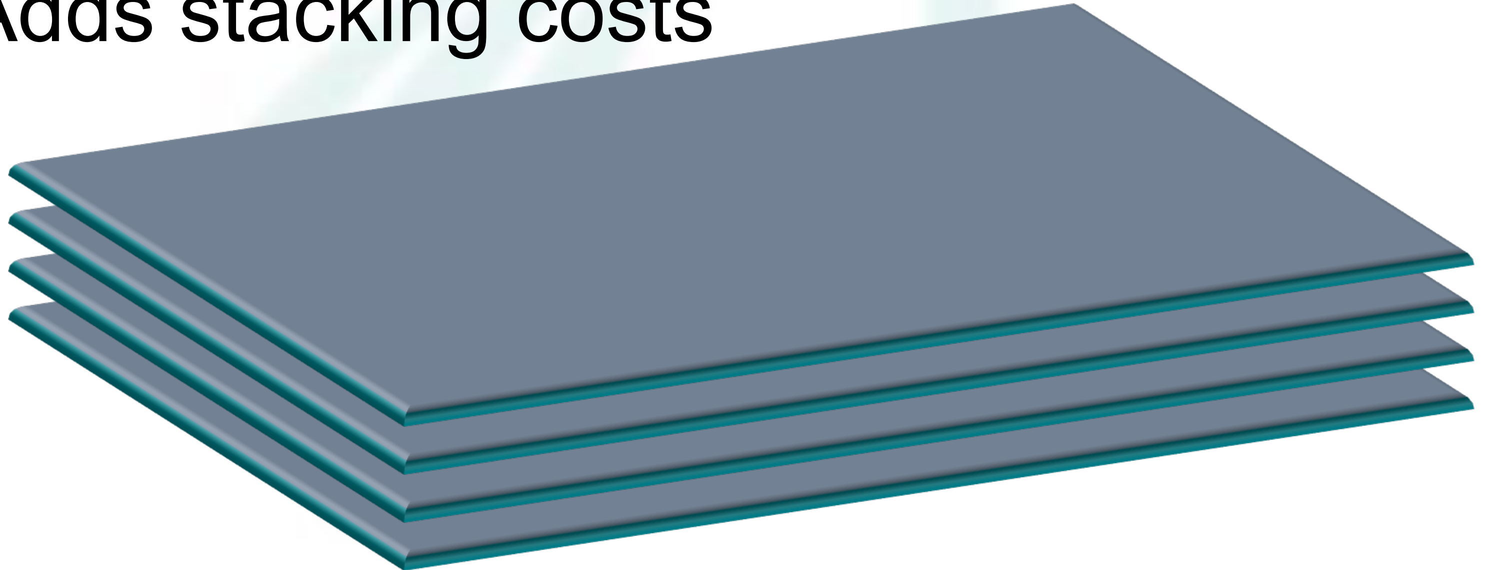
Multi Channel Memory

- Reduces Trace Lengths
- Reduces Power
- Reduces Latency
- Supports Multi Threading
- Supports Multi-Core
- Increases Bandwidth
- **Increases Transaction Rate**

Conventional 3D *Packaging*

- ***Die* Stacking**
- Preserves traditional RAM problems
- Adds stacking costs



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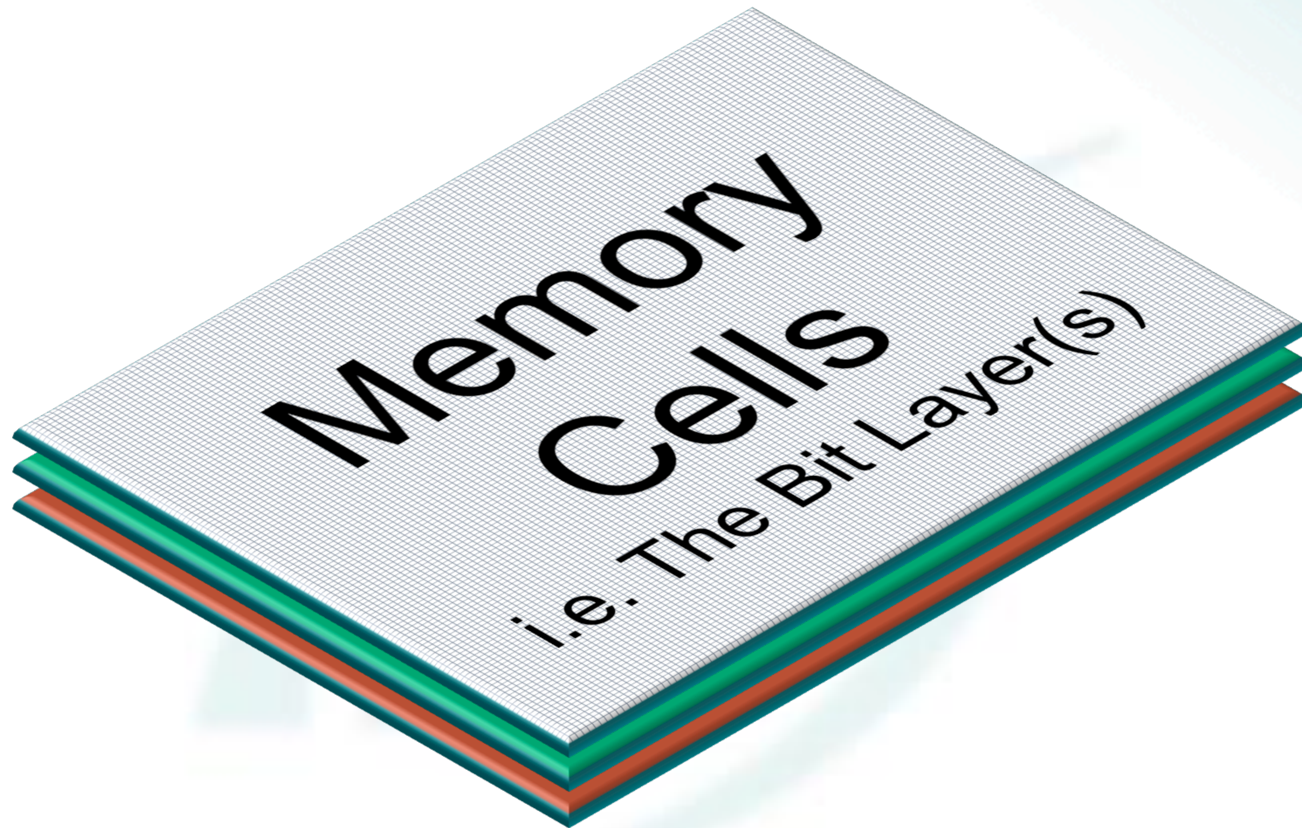
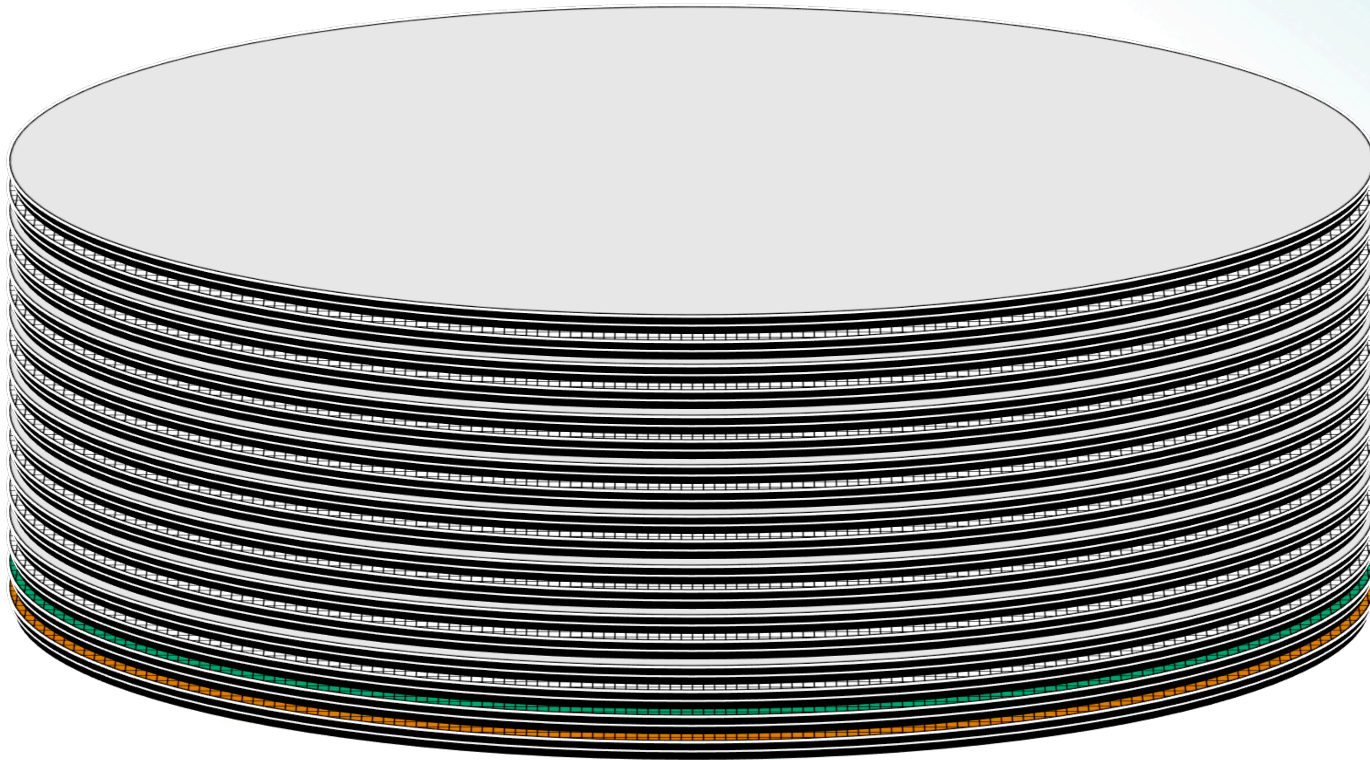
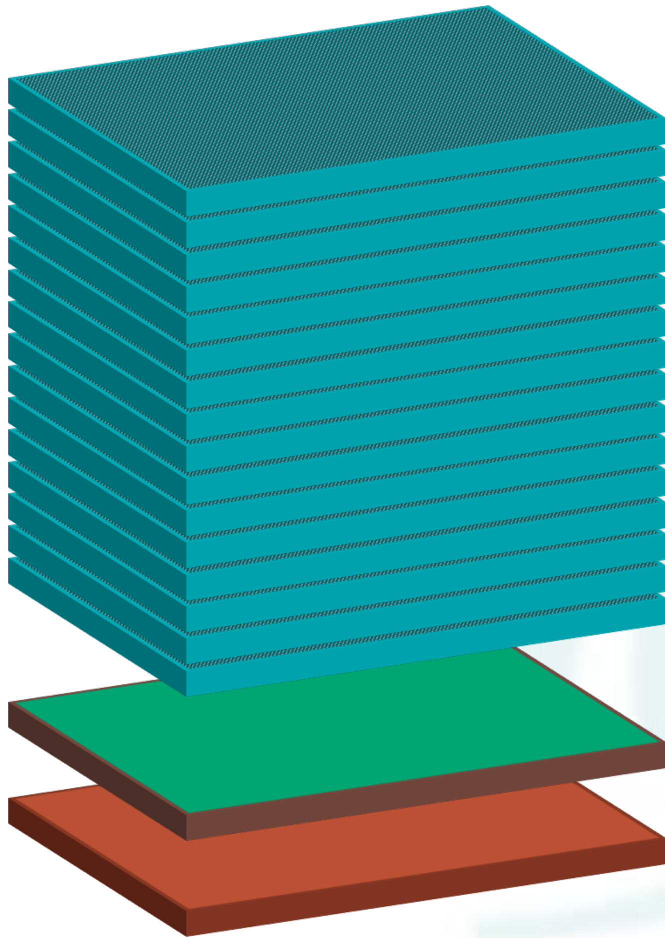
Di3D™: Dis-Integrated 3D™



Tezzaron Stacks Wafers



Dis-Integrated DiRAM4 Architecture



The Bit Layer(s)
(Memory Cells &
Access Transistors)

The Control Layer
(Sense Amps, etc.)

The I/O Layer

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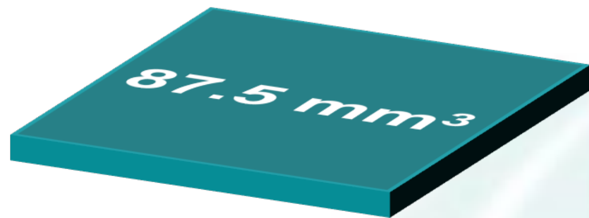
Dis-Integrated DiRAM4 Architecture

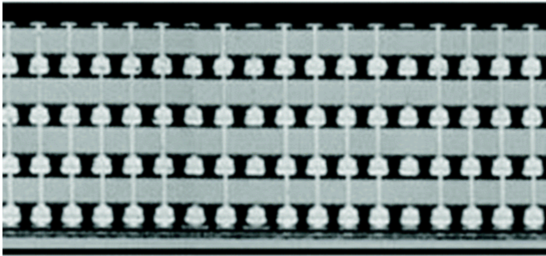


Isometric View

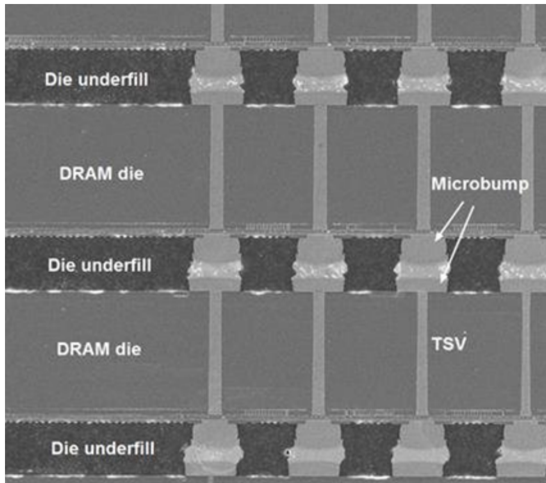
Highest Transistors Density Possible

True *Architectural* 3D

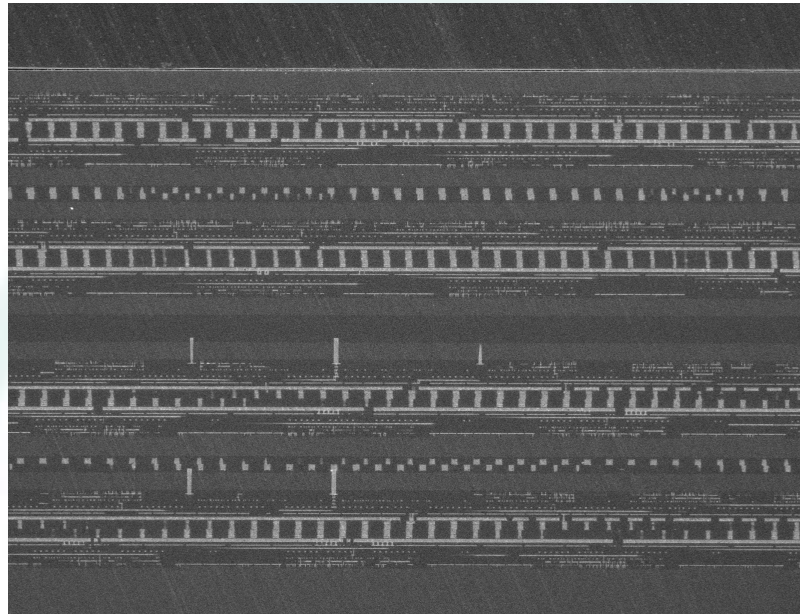
Micron HMC Die Stack



Hynix HBM Die Stack



Tezzaron TSV-free
Wafer Bonding



1st bonding: F-to-F

2nd bonding : B-to-B

1st bonding: F-to-F

3rd bonding : B-to-B

1st bonding: F-to-F

2nd bonding : B-to-B

1st bonding: F-to-F

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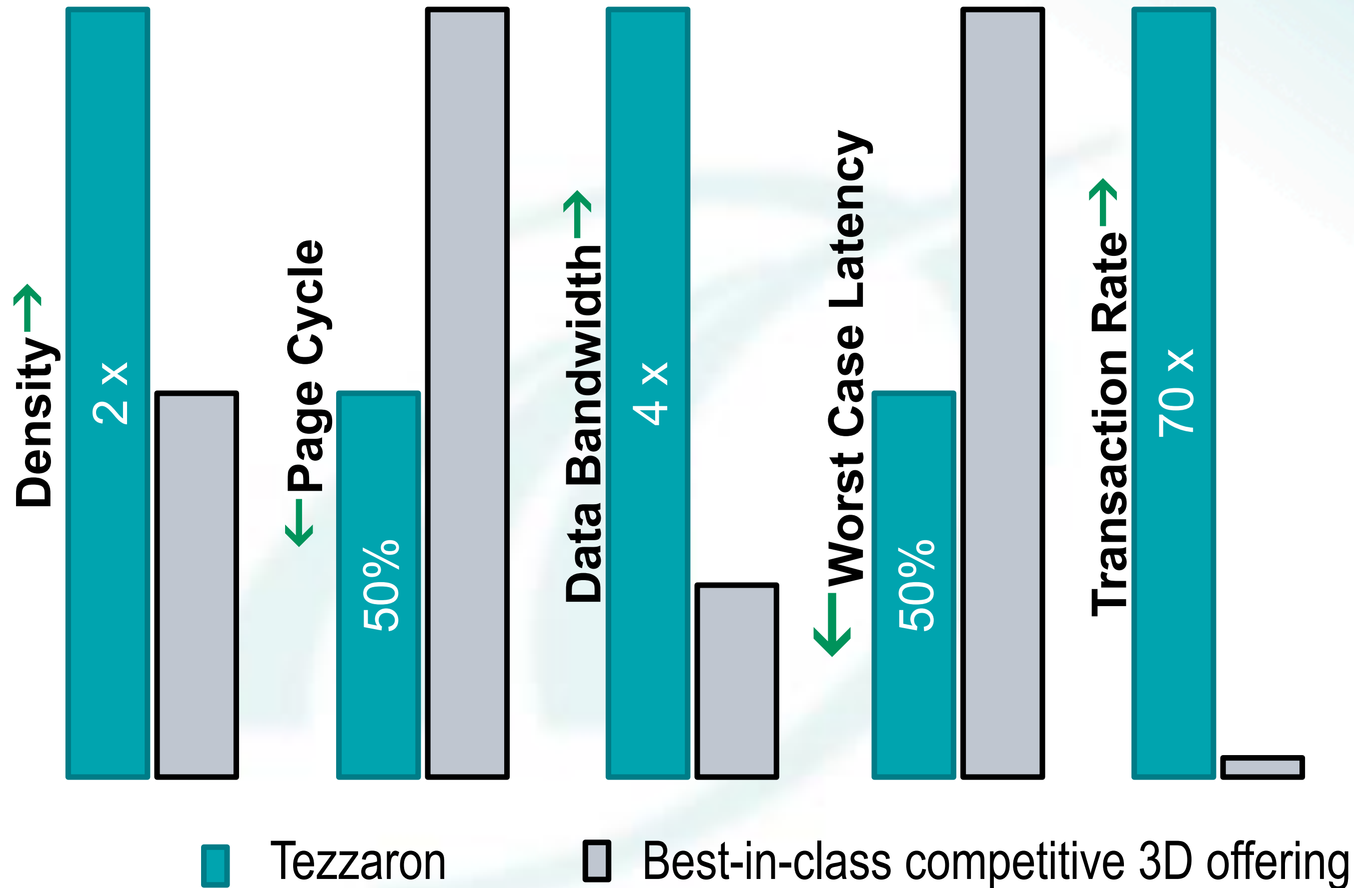
DiRAM4 Performance Advantage



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3rd Wave RAM

- High Signal Count
- Intimate Interface
- High Trans Rate
- Low Latency
- High Power Density
- Much Smarter
- **Non-commodity**

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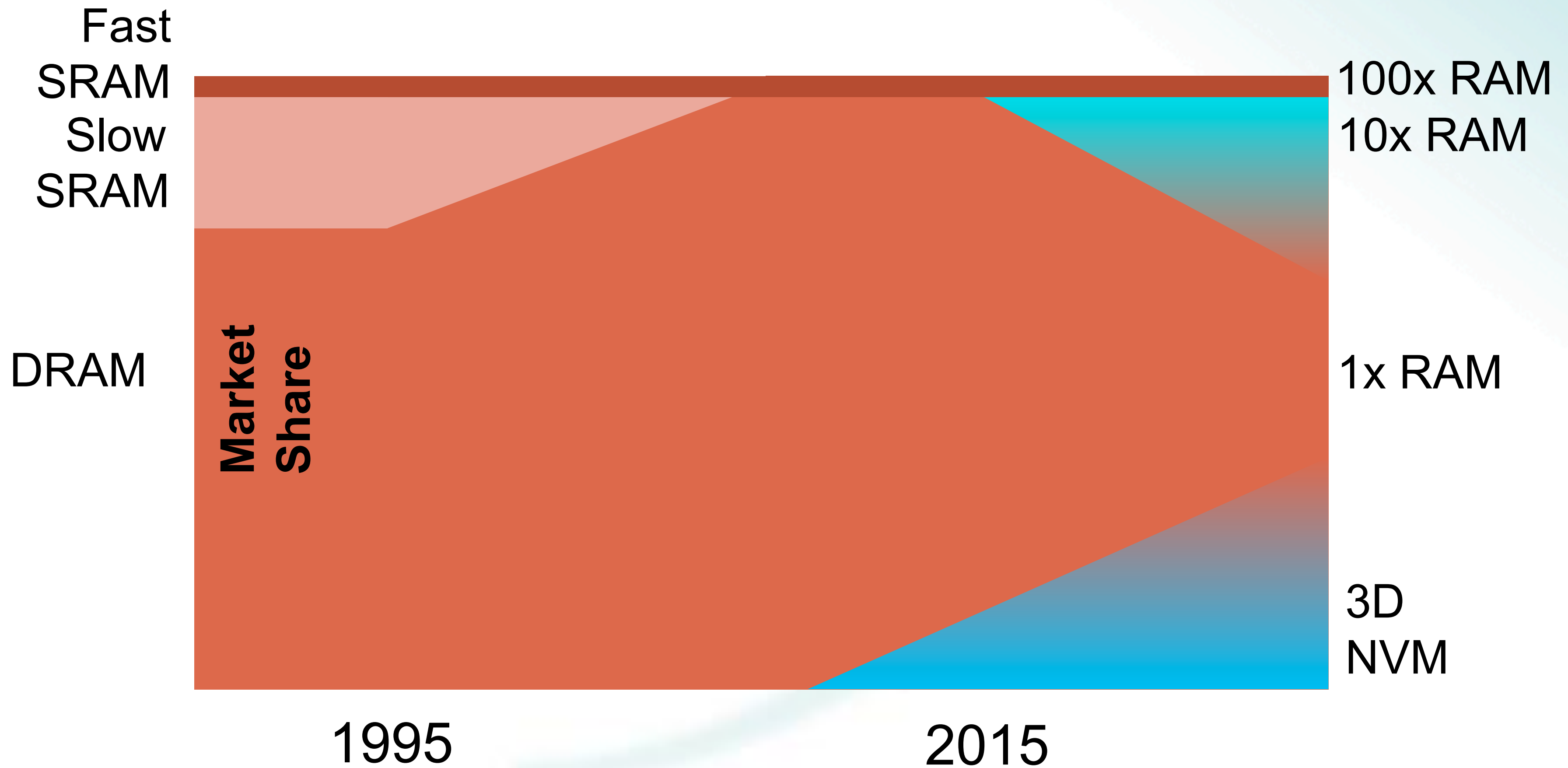
Ending the Long Boil



Crossing the Chasm…

Expect FPGA Early Adopters

- ✓ Performance driven
- ✓ Quick to market
- ✓ Small volumes
- ✓ High value

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Ayrees SyoPort-P BGA Module

Bits 0
Bits 1
Bits 2
Bits 3
Bits 4
Bits 5
Bits 6
Bits 7
Bits 8
Bits 9
Bits 10
Bits 11
Bits 12
Bits 13
Bits 14
Bits 15
Cntl
I/O-1
MHUB-1
BGA Package Substrate

I^2C Internal
SDA
SCL
SPI
SPI
I^2C External
SDA
SCL

Maintenance Port
Maintenance Port

DiRAM4
64C64
64 Ports
SIO DDR
x32 Each
4096 Data Wires

16 SIO Ports
16 SIO Ports
16 SIO Ports
16 SIO Ports

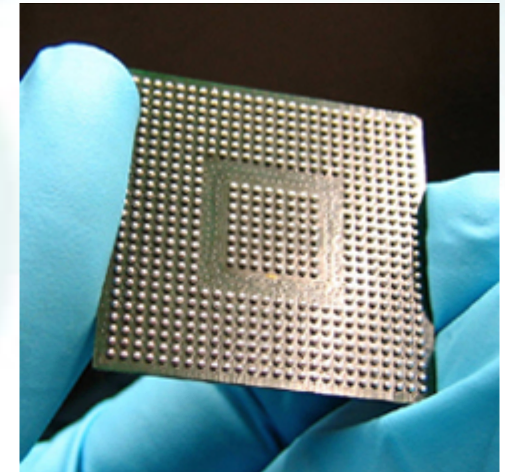
SyoPort™
Tagging
Hub
DTH1
4 Ports
SIO DDR
x64 Each
512 Add/Data Wires

x64 SIO Port
x64 SIO Port
x64 SIO Port
x64 SIO Port

JTAG Internal
JTAG (ARM)
JTAG DiRAM4
JTAG (ARM)
JTAG DTH1
JTAG External

TDO
TMS
TCK
TRST#
TDI

TDI
TMS
TCK
TRST#
TDO



http://www.etech-web.com/bga-reballing.htm

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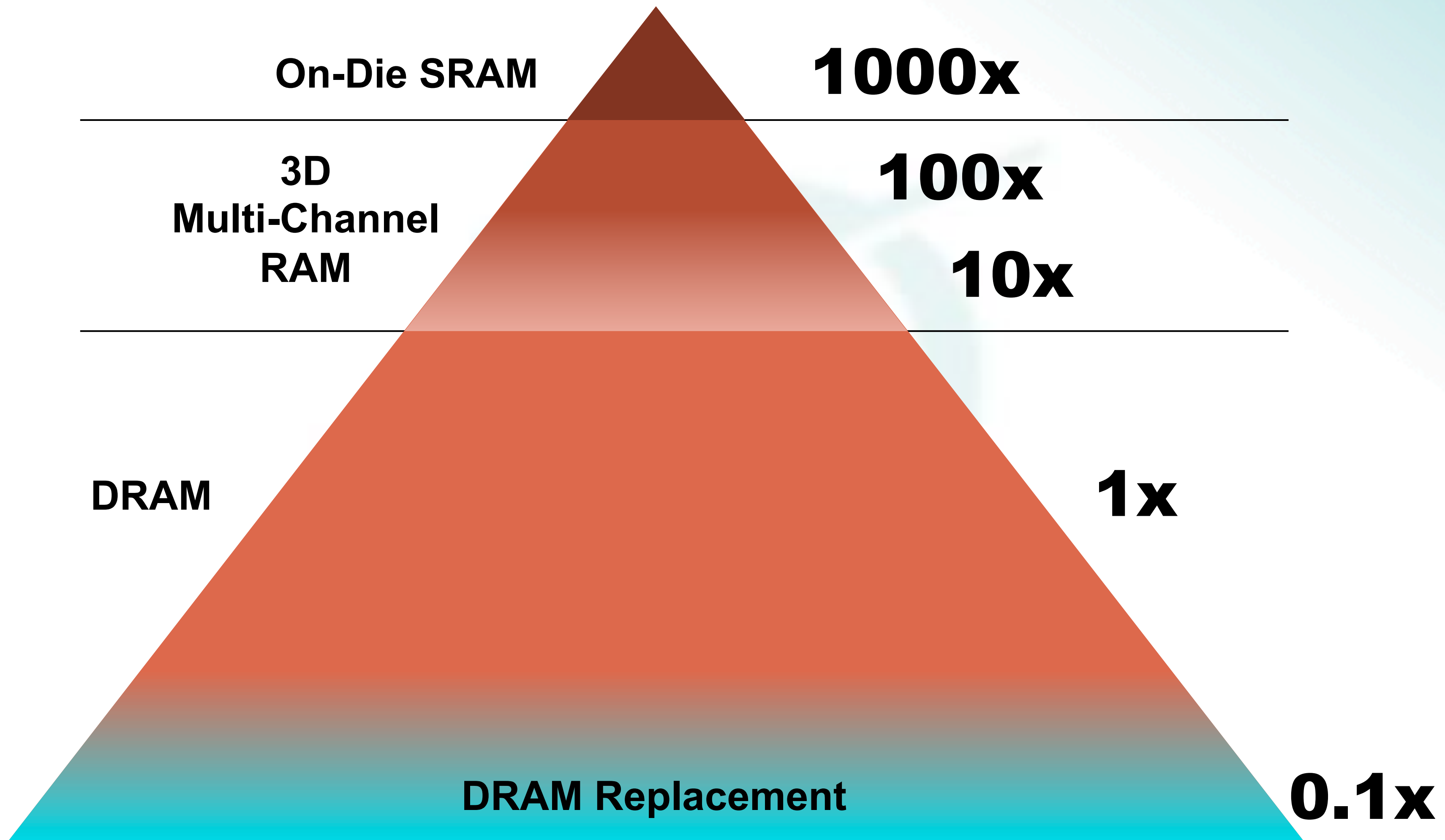
Volatile RAM Hierarchy



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Back to Normal

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The Disintegrator

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VP Marketing

512-356-2534

dchapman@tezzaron.com