IMIS™

Type: Physical

Outline # 1

Revision 1.0

Date: 6/1/2008

Surface Categories: A, B, C

Footprint Variations: A

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Introduction

This document defines a physical standard of interface characteristics for mounting memory onto any host device in a 3D configuration. The standard has been named IMIS™ (Intimate Memory Interface Specification). IMIS™ includes a system of pin definitions, specifying locations and order, made as generic as possible in order to cover a wide range of implementations. The specification also includes a set of surface preparation requirements to cover various categories of bonding methods.

This standard does not specify protocols or electrical characteristics; these must be agreed upon between the memory designer and the designer of the host device.

Pin Specifications

The port footprint measures 450µm high by 2000µm wide and contains a pin grid that is 19 cells high by 80 cells wide. Each cell is a square measuring 25µm on a side.

Pin Locations

Because the pin grid is 80 cells wide, the diagram is broken into eight tables for readability. Note that many cells are unpopulated.

Table 1: Pin Columns 0 Through 9

Pin #	0	1	2	3	4	5	6	7	8	9
		GND		GND		GND		GND		GND
	VDDQ		VDD		VDDQ		VDD		VDDQ	
	CFG0	CFG1	STBAI	GND	CLKA	GND	STBAO	ECLKA	CFG2	CFG3
Address	AI0	AO0	AI1	AO1	AI2	AO2	AI3	AO3	AI4	AO4
	DA0I0	DA0O0	DA0I1	DA0O1	DA0I2	DA0O2	DA0I3	DA0O3	DA0I4	DA0O4
Byte A										
	DA0I5	DA0O5	DA0I6	DA0O6	DA0I7	DA0O7	DA0PI	DA0PO	BWA0I	BWA0O
	DA1I0	DA1O0	DA1I1	DA1O1	DA1I2	DA1O2	DA1I3	DA1O3	DA1I4	DA1O4
Byte A’										
	DA1I5	DA1O5	DA1I6	DA1O6	DA1I7	DA1O7	DA1PI	DA1PO	BWA1I	BWA1O
	VDDQ		VDD		VDDQ		VDD		VDDQ	
		GND		GND		GND		GND		GND

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Table 2: Pin Columns 10 Through 19

Pin #	10	11	12	13	14	15	16	17	18	19
		GND		GND		GND		GND		GND
	VDD		VDDQ		VDD		VDDQ		VDD	
	RESET#	ERR#	STBEI	GND	CLKE	GND	STBEO	ECLKE	RASI	RASO
Address	AI5	AO5	AI6	AO6	AI7	AO7	AI8	AO8	AI9	AO9
	DE0I0	DE0O0	DE0I1	DE0O1	DE0I2	DE0O2	DE0I3	DE0O3	DE0I4	DE0O4
Byte E										
	DE0I5	DE0O5	DE0I6	DE0O6	DE0I7	DE0O7	DE0PI	DE0PO	BWE0I	BWE0O
	DE1I0	DE1O0	DE1I1	DE1O1	DE1I2	DE1O2	DE1I3	DE1O3	DE1I4	DE1O4
Byte E'										
	DE1I5	DE1O5	DE1I6	DE1O6	DE1I7	DE1O7	DE1PI	DE1PO	BWE1I	BWE1O
	VDD		VDDQ		VDD		VDDQ		VDD	
		GND		GND		GND		GND		GND

Table 3: Pin Columns 20 Through 29

Pin #	20	21	22	23	24	25	26	27	28	29
		GND		GND		GND		GND		GND
	VDDQ		VDD		VDDQ		VDD		VDDQ	
	CASI	CASO	STBCI	GND	CLKC	GND	STBCO	ECLKC	CTYPI0	CTYPI1
Address	AI10	AO10	AI11	AO11	AI12	AO12	AI13	AO13	AI14	AO14
	DC0I0	DC0O0	DC0I1	DC0O1	DC0I2	DC0O2	DC0I3	DC0O3	DC0I4	DC0O4
Byte C										
	DC0I5	DC0O5	DC0I6	DC0O6	DC0I7	DC0O7	DC0PI	DC0PO	CWC0I	CWC0O
	DC1I0	DC1O0	DC1I1	DC1O1	DC1I2	DC1O2	DC1I3	DC1O3	DC1I4	DC1O4
Byte C'										
	DC1I5	DC1O5	DC1I6	DC1O6	DC1I7	DC1O7	DC1PI	DC1PO	CWC1I	CWC1O
	VDDQ		VDD		VDDQ		VDD		VDDQ	
		GND		GND		GND		GND		GND

Table 4: Pin Columns 30 Through 39

Pin #	30	31	32	33	34	35	36	37	38	39
		GND		GND		GND		GND		GND
	VDD		VDDQ		VDD		VDDQ		VDD	
	CTYPI2	CTYPI3	STBFI	GND	CLKF	GND	STBFO	ECLKF	CTYPO0	CTYPO1
Address	AI15	AO15	AI16	AO16	AI17	AO17	AI18	AO18	AI19	AO19
	DF0I0	DF0O0	DF0I1	DF0O1	DF0I2	DF0O2	DF0I3	DF0O3	DF0I4	DF0O4
Byte F										
	DF0I5	DF0O5	DF0I6	DF0O6	DF0I7	DF0O7	DF0PI	DF0PO	BWF0I	BWF0O
	DF1I0	DF1O0	DF1I1	DF1O1	DF1I2	DF1O2	DF1I3	DF1O3	DF1I4	DF1O4
Byte F'										
	DF1I5	DF1O5	DF1I6	DF1O6	DF1I7	DF1O7	DF1PI	DF1PO	BWF1I	BWF1O
	VDD		VDDQ		VDD		VDDQ		VDD	
		GND		GND		GND		GND		GND

Table 5: Pin Columns 40 Through 49

Pin #	40	41	42	43	44	45	46	47	48	49
		GND		GND		GND		GND		GND
	VDDQ		VDD		VDDQ		VDD		VDDQ	
	CTYPO2	CTYPO3	STBBI	GND	CLKB	GND	STBBO	ECLKB	BIA0	BOA0
Address	AI20	AO20	AI21	AO21	AI22	AO22	AI23	AO23	AI24	AO24
	DB0I0	DB0O0	DB0I1	DB0O1	DB0I2	DB0O2	DB0I3	DB0O3	DB0I4	DB0O4
Byte B										
	DB0I5	DB0O5	DB0I6	DB0O6	DB0I7	DB0O7	DB0PI	DB0PO	BWB0I	BWB0O
	DB1I0	DB1O0	DB1I1	DB1O1	DB1I2	DB1O2	DB1I3	DB1O3	DB1I4	DB1O4
Byte B'										
	DB1I5	DB1O5	DB1I6	DB1O6	DB1I7	DB1O7	DB1PI	DB1PO	BWB1I	BWB1O
	VDDQ		VDD		VDDQ		VDD		VDDQ	
		GND		GND		GND		GND		GND

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Table 6: Pin Columns 50 Through 59

Pin #	50	51	52	53	54	55	56	57	58	59
		GND		GND		GND		GND		GND
	VDD		VDDQ		VDD		VDDQ		VDD	
	BIA1	BOA1	STBGI	GND	CLKG	GND	STBGO	ECLKG	BIA2	BOA2
Address	AI25	AO25	AI26	AO26	AI27	AO27	AI28	AO28	AI29	AO29
	DG0I0	DG0O0	DG0I1	DG0O1	DG0I2	DG0O2	DG0I3	DG0O3	DG0I4	DG0O4
Byte G										
	DG0I5	DG0O5	DG0I6	DG0O6	DG0I7	DG0O7	DG0PI	DG0PO	BWG0I	BWG0O
	DG1I0	DG1O0	DG1I1	DG1O1	DG1I2	DG1O2	DG1I3	DG1O3	DG1I4	DG1O4
Byte G'										
	DG1I5	DG1O5	DG1I6	DG1O6	DG1I7	DG1O7	DG1PI	DG1PO	BWG1I	BWG1O
	VDD		VDDQ		VDD		VDDQ		VDD	
		GND		GND		GND		GND		GND

Table 7: Pin Columns 60 Through 69

Pin #	60	61	62	63	64	65	66	67	68	69
		GND		GND		GND		GND		GND
	VDDQ		VDD		VDDQ		VDD		VDDQ	
	BIA3	BOA3	STBDI	GND	CLKD	GND	STBDO	ECLKD	BIA4	BOA4
Address	AI30	AO30	AI31	AO31	AI32	AO32	AI33	AO33	AI34	AO34
	DD0I0	DD0O0	DD0I1	DD0O1	DD0I2	DD0O2	DD0I3	DD0O3	DD0I4	DD0O4
Byte D										
	DD0I5	DD0O5	DD0I6	DD0O6	DD0I7	DD0O7	DD0PI	DD0PO	BWD0I	BWD0O
	DD1I0	DD1O0	DD1I1	DD1O1	DD1I2	DD1O2	DD1I3	DD1O3	DD1I4	DD1O4
Byte D'										
	DD1I5	DD1O5	DD1I6	DD1O6	DD1I7	DD1O7	DD1PI	DD1PO	BBWD1I	BWD1O
	VDDQ		VDD		VDDQ		VDD		VDDQ	
		GND		GND		GND		GND		GND

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Table 8: Pin Columns 70 Through 79

Pin #	70	71	72	73	74	75	76	77	78	79
		GND		GND		GND		GND		GND
	VDD		VDDQ		VDD		VDDQ		VDD	TDOUT
	BIA5	BOA5	STBHI	GND	CLKH	GND	STBHO	ECLKH	SDA/TDIN	SCK/TCLK
Address	AI35	AO35	AI36	AO36	AI37	AO37	AI38	AO38	AI39	AO39
Byte H	DH0I0	DH0O0	DH0I1	DH0O1	DH0I2	DH0O2	DH0I3	DH0O3	DH0I4	DH0O4
	DH0I5	DH0O5	DH0I6	DH0O6	DH0I7	DH0O7	DH0PI	DH0PO	BWH0I	BWH0O
Byte H’	DH1I0	DH1O0	DH1I1	DH1O1	DH1I2	DH1O2	DH1I3	DH1O3	DH1I4	DH1O4
	DH1I5	DH1O5	DH1I6	DH1O6	DH1I7	DH1O7	DH1PI	DH1PO	BWH1I	BWH1O
	VDD		VDDQ		VDD		VDDQ		VDD	
		GND		GND		GND		GND		GND

Pin Descriptions

Name	Type	Description
AIx	I	Address for input data
AOx	I	Address for output data or single address modes
D(A-H)(0-1)Ix	I/O	Data input
D(A-H)(0-1)Ox	I/O	Data output or output/input for BiDirectional data
CFGx	I	Hard wired configuration bits
RESET#	I	Reset
STB(A-H)I	I	Input data strobe
STB(A-H)O	O	Output data strobe
ECLK(A-H)	O	Echo clock output in phase with data
ERR#	O	Uncorrectable ECC error occurred on current read data
CLK(A-H)	I	Data Transfer CLK
BW(A-H)(0-1)I	I	Byte write enable for D(A-H)(0-1)(I,O)x
BW(A-H)(0-1)O	I/O	Reserved
CTYPI(3-0)	I	Input cycle type controls
CTYPO(3-0)	I	Output cycle type controls
RASI	I	RAS input cycles
CASI	I	CAS input cycles
RASO	I	RAS output cycles or single address modes
CASO	I	CAS output cycles or single address modes
BIA(5-0)	I	Bank address, input address related
BOA(5-0)	I	Bank address, output address related or for single address modes
SDA	I/O	Data pin; I2C device link for test and configuration
SCK	I	Clock pin; I2C device link for test and configuration
TCLK	I	Test Access Port (TAP) Clock
TDIN	I	Test Access Port (TAP) Data In
TDOUT	O	Test Access Port (TAP) Data Out

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Pin Usage by Memory Type

SDR DRAM, DDR DRAM, and DDR Flash

Pin Name	Usage
AIx	N/C
AOx	Address
D(A-H)(0-1)Ix	Data Input Unidirectional Bus Mode
D(A-H)(0-1)Ox	Data BiDi Mode/Data Output Unidirectional Bus Mode
CFG0	1=Mux Address
CFG1	No connect
CFG2	No connect
CFG3	No connect
RESET#	Reset#
STB(A-H)I	Input Data Strobe by Byte
STB(A-H)O	Output Data Strobe by Byte
ECLK(A-H)	No connect
ERR#	ERR#
CLK(A-B, D-H)	Optional Byte Clk
CLKC	Clk/Opt. Byte C Clk
BW(A-H)(0-1)I	DM
BW(A-H)(0-1)O	Reserved
CTYPI0	No connect
CTYPI1	No connect
CTYPI2	No connect
CTYPI3	No connect
CTYPO0	WR#
CTYPO1	CKE
CTYPO2	CS#
CTYPO3	ODT
RASI	No connect
CASI	No connect
RASO	RAS#
CASO	CAS#
BIA(5-0)	No connect
BOA(5-0)	Bank Addresses
SDA	Data pin; I2C device link for test and configuration
SCK	Clock pin; I2C device link for test and configuration
TCLK	Test Access Port (TAP) Clock
TDIN	Test Access Port (TAP) Data In
TDOUT	Test Access Port (TAP) Data Out

QTR DRAM

Pin Name	Usage
AIx	Address (split Opt)
AOx	Address
D(A-H)(0-1)Ix	Data Input Unidirectional Bus Mode
D(A-H)(0-1)Ox	Data BiDi Mode/Data Output Unidirectional Bus Mode
CFG0	1=Mux Address
CFG1	No connect
CFG2	No connect
CFG3	No connect
RESET#	Reset#
STB(A-H)I	Input Data Strobe by Byte
STB(A-H)O	Output Data Strobe by Byte
ECLK(A-H)	No connect
ERR#	ERR#
CLK(A-B, D-H)	Optional Byte Clk
CLKC	Clk/Opt. Byte C Clk
BW(A-H)(0-1)I	DM
BW(A-H)(0-1)O	Reserved
CTYPI0	No connect
CTYPI1	No connect
CTYPI2	No connect
CTYPI3	No connect
CTYPO0	WR#
CTYPO1	CKE
CTYPO2	CS#
CTYPO3	ODT
RASI	No connect
CASI	No connect
RASO	RAS#
CASO	CAS#
BIA(5-0)	No connect
BOA(5-0)	Bank Addresses
SDA	Data pin; I2C device link for test and configuration
SCK	Clock pin; I2C device link for test and configuration
TCLK	Test Access Port (TAP) Clock
TDIN	Test Access Port (TAP) Data In
TDOUT	Test Access Port (TAP) Data Out

NBT SRAM

Pin Name	Usage
AIx	No connect
AOx	Address
D(A-H)(0-1)Ix	Data Input Unidirectional Bus Mode
D(A-H)(0-1)Ox	Data BiDi Mode/Data Output Unidirectional Bus Mode
CFG0	No connect
CFG1	LBO#
CFG2	No connect
CFG3	No connect
RESET#	Reset#
STB(A-H)I	No connect
STB(A-H)O	No connect
ECLK(A-H)	Echo Clk Output
ERR#	ERR#
CLK(A-B, D-H)	Optional Byte Clk
CLKC	Opt Clk/Opt. Byte C Clk
BW(A-H)(0-1)I	BW
BW(A-H)(0-1)O	Reserved
CTYPI0	No connect
CTYPI1	No connect
CTYPI2	No connect
CTYPI3	OE#
CTYPO0	WR#
CTYPO1	CKE#
CTYPO2	CS#
CTYPO3	ADV / LD#
RASI	No connect
CASI	No connect
RASO	Clk
CASO	No connect
BIA(5-0)	No connect
BOA(5-0)	No connect
SDA	Data pin; I2C device link for test and configuration
SCK	Clock pin; I2C device link for test and configuration
TCLK	Test Access Port (TAP) Clock
TDIN	Test Access Port (TAP) Data In
TDOUT	Test Access Port (TAP) Data Out

DTR SRAM and QTR SRAM

Pin Name	Usage
AIx	Address (split Opt)
AOx	Address
D(A-H)(0-1)Ix	Data Input Unidirectional Bus Mode
D(A-H)(0-1)Ox	Data BiDi Mode/Data Output Unidirectional Bus Mode
CFG0	No connect
CFG1	DLL OFF#
CFG2	No connect
CFG3	No connect
RESET#	Reset#
STB(A-H)I	No connect
STB(A-H)O	Negative Echo Clk Output (C#)
ECLK(A-H)	Positive Echo Clk Output (C)
ERR#	ERR#
CLK(A-B, D-H)	Optional Byte Clk
CLKC	Opt Clk/Opt. Byte C Clk
BW(A-H)(0-1)I	BW
BW(A-H)(0-1)O	QVLD (A-H) (0-1)
CTYPI0	No connect
CTYPI1	No connect
CTYPI2	No connect
CTYPI3	No connect
CTYPO0	WPS# / R / W#
CTYPO1	No connect
CTYPO2	RPS# / LD#
CTYPO3	No connect
RASI	No connect
CASI	No connect
RASO	K
CASO	Kbar
BIA(5-0)	No connect
BOA(5-0)	No connect
SDA	Data pin; I2C device link for test and configuration
SCK	Clock pin; I2C device link for test and configuration
TCLK	Test Access Port (TAP) Clock
TDIN	Test Access Port (TAP) Data In
TDOUT	Test Access Port (TAP) Data Out

Dual Port

Pin Name	Usage
AIx	Address Port B
AOx	Address Port A
D(A-H)(0-1)Ix	Port B Data
D(A-H)(0-1)Ox	Port A Data
CFG0	No connect
CFG1	DLL OFF#
CFG2	No connect
CFG3	No connect
RESET#	Reset#
STB(A-H)I	Echo Clk Port B
STB(A-H)O	Echo Clk Port A
ECLK(A-H)	No connect
ERR#	ERR#
CLK(A-B, D-H)	Optional Byte Clk
CLKC	Opt Clk/Opt. Byte C Clk
BW(A-H)(0-1)I	BW Port B
BW(A-H)(0-1)O	BW Port A
CTYPI0	Port B: WR# or WPS#
CTYPI1	No connect
CTYPI2	Port B: CS# or RPS#
CTYPI3	No connect
CTYPO0	Port A: WR# or WPS#
CTYPO1	No connect
CTYPO2	Port A: CS# or RPS#
CTYPO3	No connect
RASI	K Port B
CASI	Kbar Port B
RASO	K Port A
CASO	Kbar Port A
BIA(5-0)	No connect
BOA(5-0)	No connect
SDA	Data pin; I2C device link for test and configuration
SCK	Clock pin; I2C device link for test and configuration
TCLK	Test Access Port (TAP) Clock
TDIN	Test Access Port (TAP) Data In
TDOUT	Test Access Port (TAP) Data Out

Surface and Target Requirements

Category A – Direct Bond Interconnect (Ziptronix DBI®)

This section describes the preferred surface configuration to facilitate mounting of the Intimate Memory onto any host device in a 3D configuration with Direct Bond Interconnect technology.

Form Factor

Semi-standard 150mm or 200mm wafers. 300mm wafers can be accommodated by coring to 150mm or 200mm.

Bow and Warp

Semi-standard

Back-End-of-Line (BEOL)

Aluminum or Copper

Surface Configuration

Exposed tungsten filled vias through silicon oxide or oxy-nitride surface passivation to host device Last Metal (Aluminum BEOL) or silicon oxide or oxy-nitride surface passivation on host device Last Metal (Copper BEOL).

Exposed electrical connections

Aluminum BEOL

15 x 15 um^2 Port Area centered within 25 x 25 um^2 cell.

An array of exposed tungsten plugs enclosed within 15 x 15 um^2 Port Area.

Minimum exposed tungsten plug area of 10 um^2.

Port Area surrounded by 10 um annulus of silicon oxide or oxy-nitride.

Copper BEOL

15 x 15 um^2 Port Area centered within 25 x 25 um^2 cell.

Last Metal covered with nominally 50 nm of silicon oxide or oxy-nitride enclosed within 15 x 15 um^2 Port Area.

Last Metal area of 100 um^2 centered within Port Area.

Port Area surrounded by 10 um annulus of silicon oxide or oxy-nitride.

No exposed copper.

Surface Planarity

0.25 microns / 25 microns

1.0 microns or less total topography variation

Test Pads (Optional)

Aluminum BEOL

Metal – Aluminum or Aluminum:Cu

Thickness – 0.5 micron

Port Area Overlap – 5 microns

Spacing – 5 microns

Post-Test Disposition – Removed prior to DBI® fabrication if within 0.5mm of DBI® interconnections or probe damage topography is greater than 1.0 microns

Copper BEOL

Metal – Aluminum or Aluminum:Cu

Thickness – 0.1 micron

Port Area Enclosure – 5 microns

Spacing – 5 microns

Last Metal Contact Cut – Cross with 5 micron long, 2 micron wide legs, centered in Port Area

Last Metal Enclosure of Contact Cut – 2.5 microns

Test Pad Enclosure of Contact Cut – 7.5 microns

Probe Portion of Test Pad from Contact Cut – 25 microns

Probed Pad Post-Test Disposition – Removed prior to DBI® fabrication if within 0.5mm of DBI® interconnections or if probe damage topography is greater than 1.0 microns

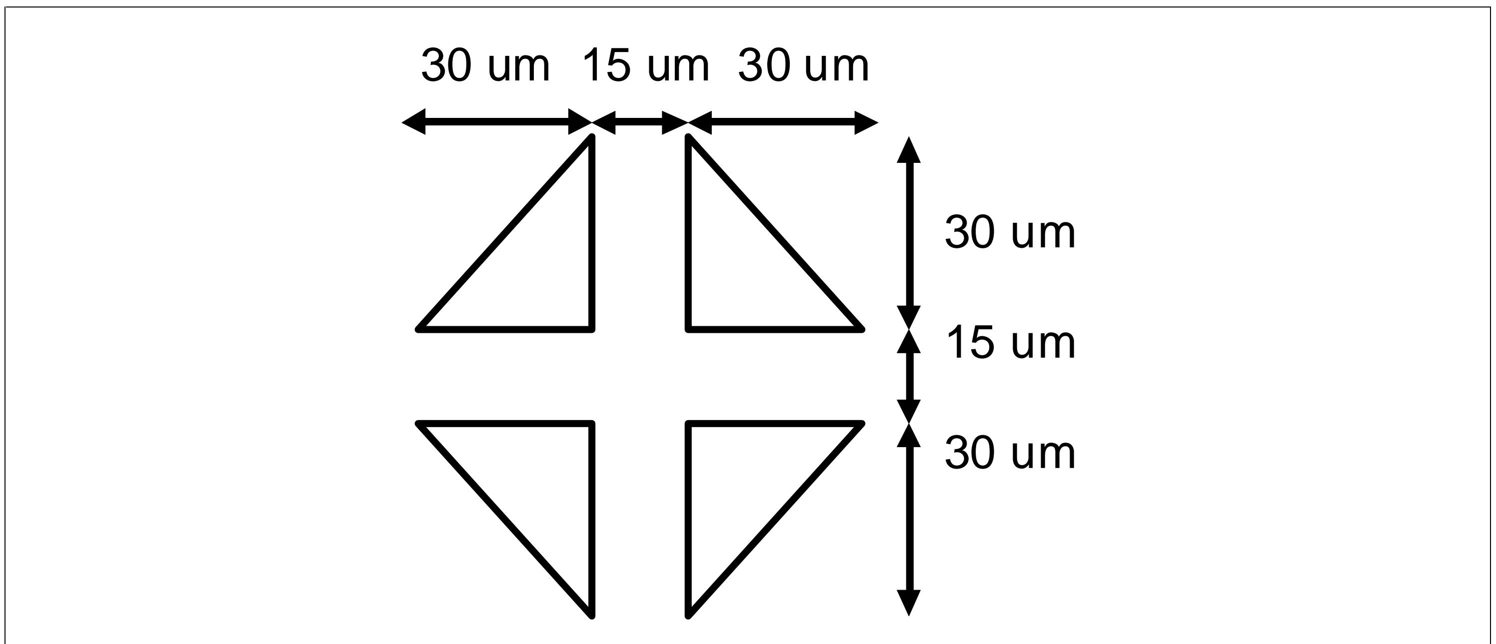
Field Size

Maximum – 40mm x 20mm (X x Y)

Minimum – 20mm x 10mm (X x Y)

DBI® Metal Alignment Targets
(on Host and Memory Device or fabricated at Ziptronix prior to DBI® fab)

Shape



Topography

0.3 microns into silicon oxide or oxy-nitride

Minimum Separation from Port Area

100 microns

Number / Field

2

Location

Horizontally spaced, within Field

Minimum Center-to-Center Separation to Other Target

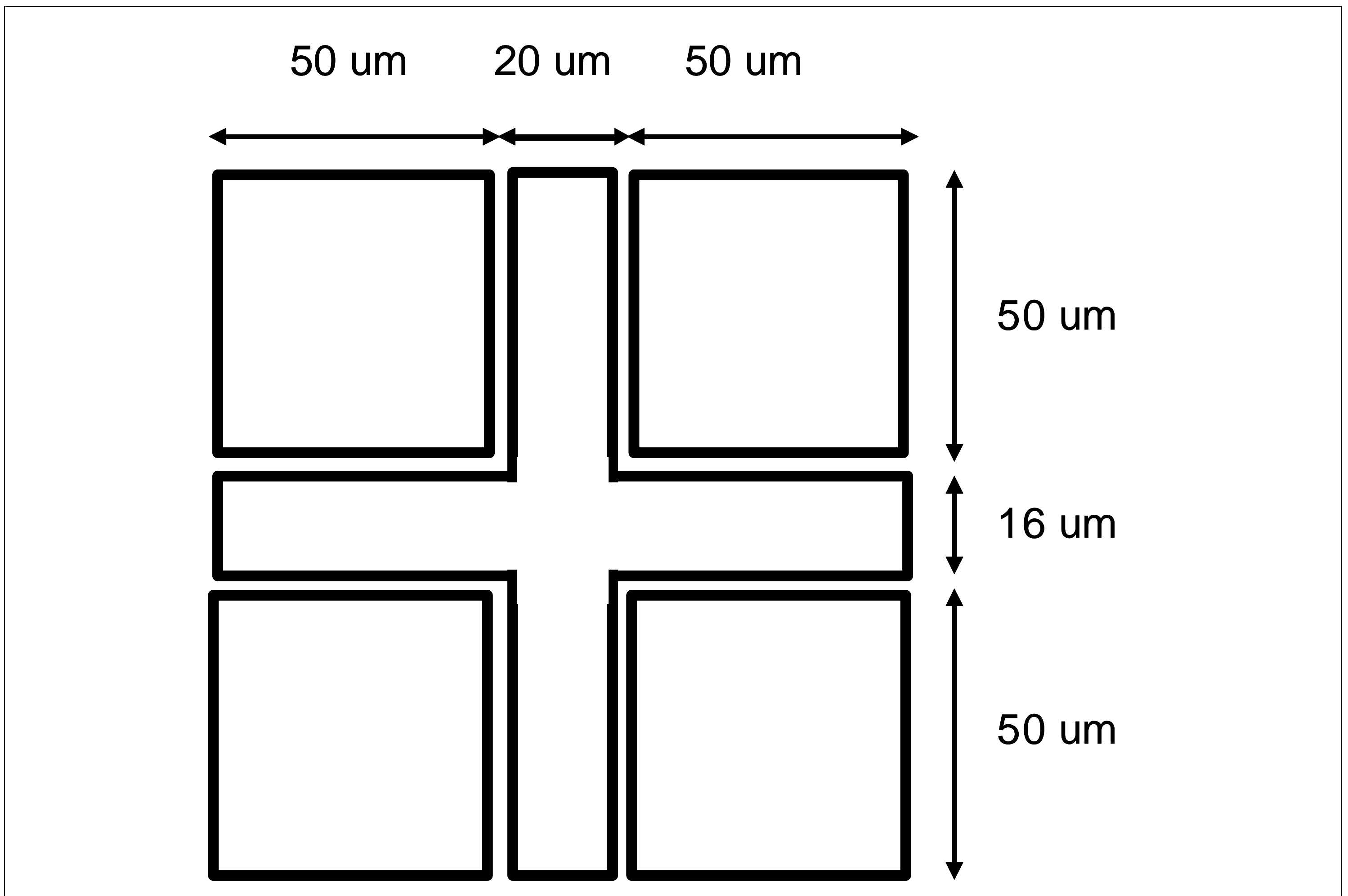
19.9 mm

Maximum Center-to-Center Separation to Other Target

Field width - 0.5 mm

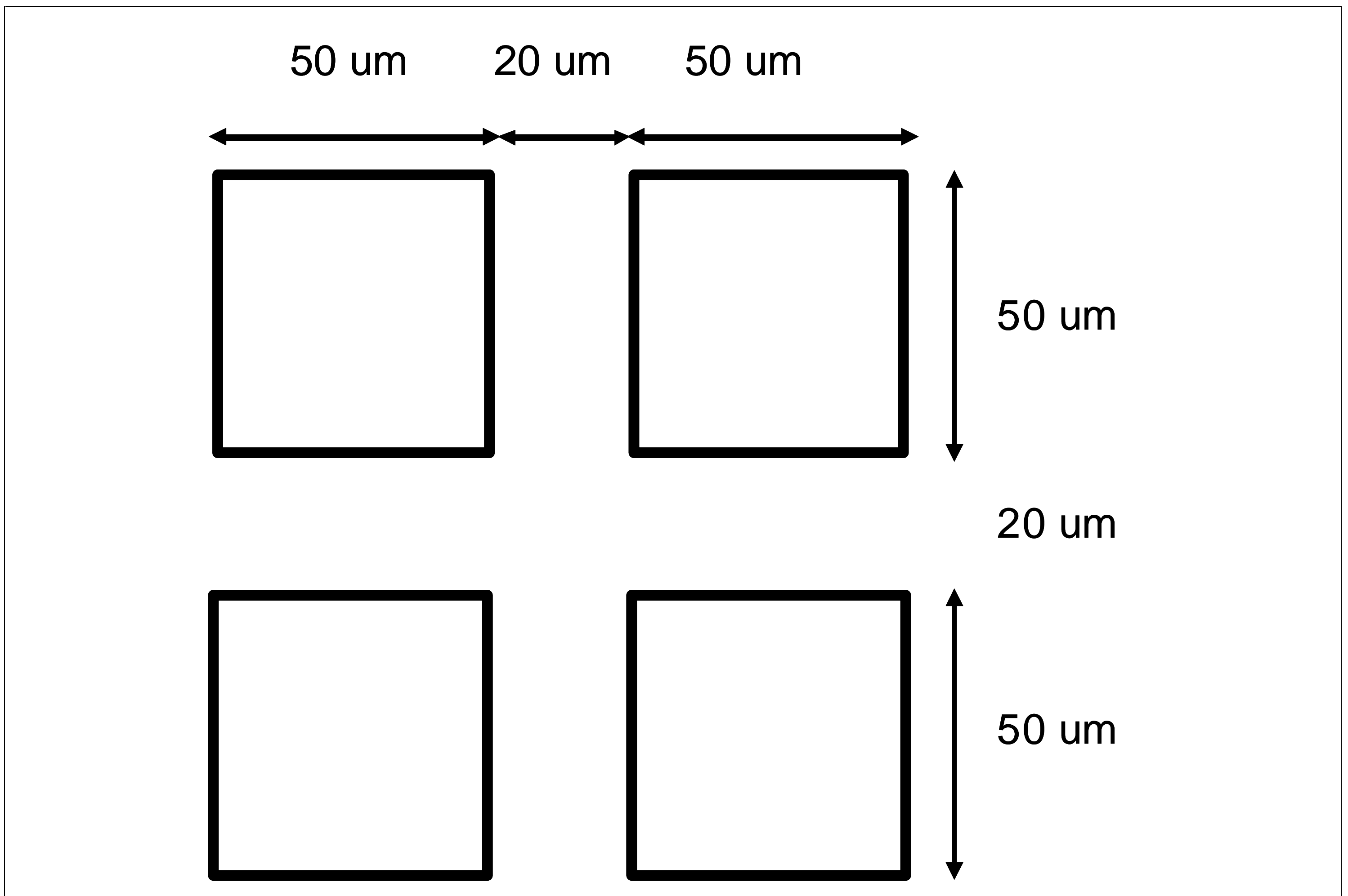
DBI® Bond Alignment Targets
(on Host and Memory Device or fabricated at Ziptronix prior to DBI® fab)

Shape Donor and Host (After Bonding)



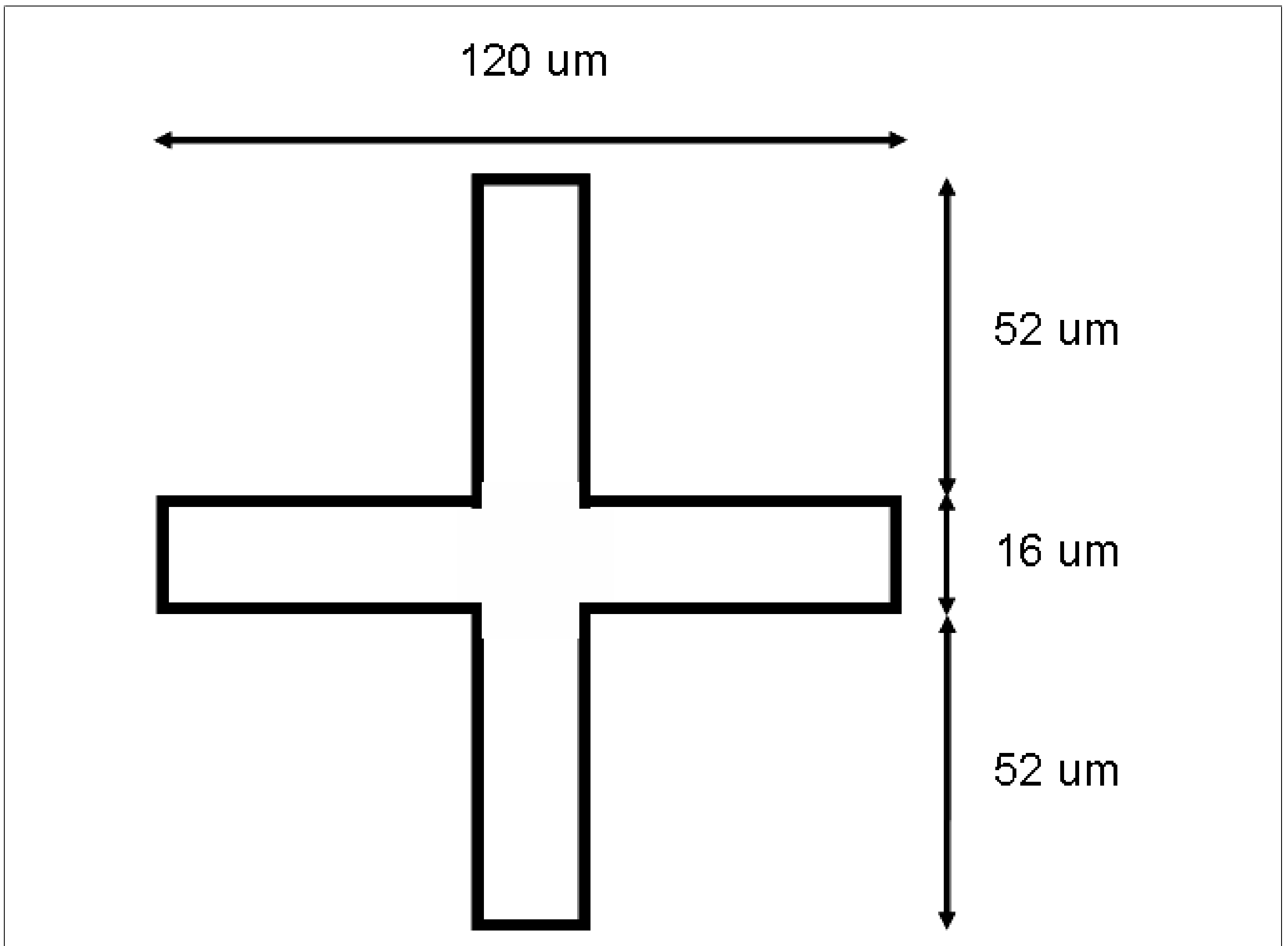
DBI® Bond Alignment Targets
(on Host Device or fabricated at Ziptronix prior to DBI® fab)

Shape Host (Before Bonding)



DBI® Bond Alignment Targets
(on Memory Device or fabricated at Ziptronix prior to DBI® fab)

Shape Donor (Before Bonding)



DBI® Bond Alignment Targets

Topography

0.3 microns into silicon oxide or oxy-nitride

Minimum Separation from Port Area

100 microns

Wafer-to-Wafer Bonding

Number Targets / Field: 2 pair / Field

Location: Horizontally spaced, within Field

Minimum Separation to Other Target: 0.5 mm

Die-to-Wafer Bonding

Number / Field – Wafer-to-Wafer Bonding: 3 pair / die

Location: 3 of 4 die corners, vertically and horizontally aligned

Minimum Separation to Other Target: 0.5 mm

Post-Bond Alignment Targets (contact mask)

Location

Optical Alignment – A minimum of two marks on the far left and right hand sides of the wafer, at the same y coordinate and within 10 mm of the x-axis wafer centerline, and greater than 10 mm but no more than 50 mm from the wafer edge.

Infrared Alignment – A minimum of two marks on the far left and right hand sides of the wafer, at the same y coordinate and within 5 mm of the x-axis wafer centerline, and greater than 15 mm and less than 30 mm from the wafer edge.

Die-to-Wafer Bonding

Pad cut – Dielectric etch to last metal on host wafer, Optical Alignment.

Wafer-to-Wafer Bonding

Dielectric cut – Silicon etch to field oxide on donor die, Infrared Alignment

Requires no metal on either wafer above or below mark.

Pad cut – Dielectric etch to first metal on donor die, Optical Alignment

Must be revealed by dielectric cut.

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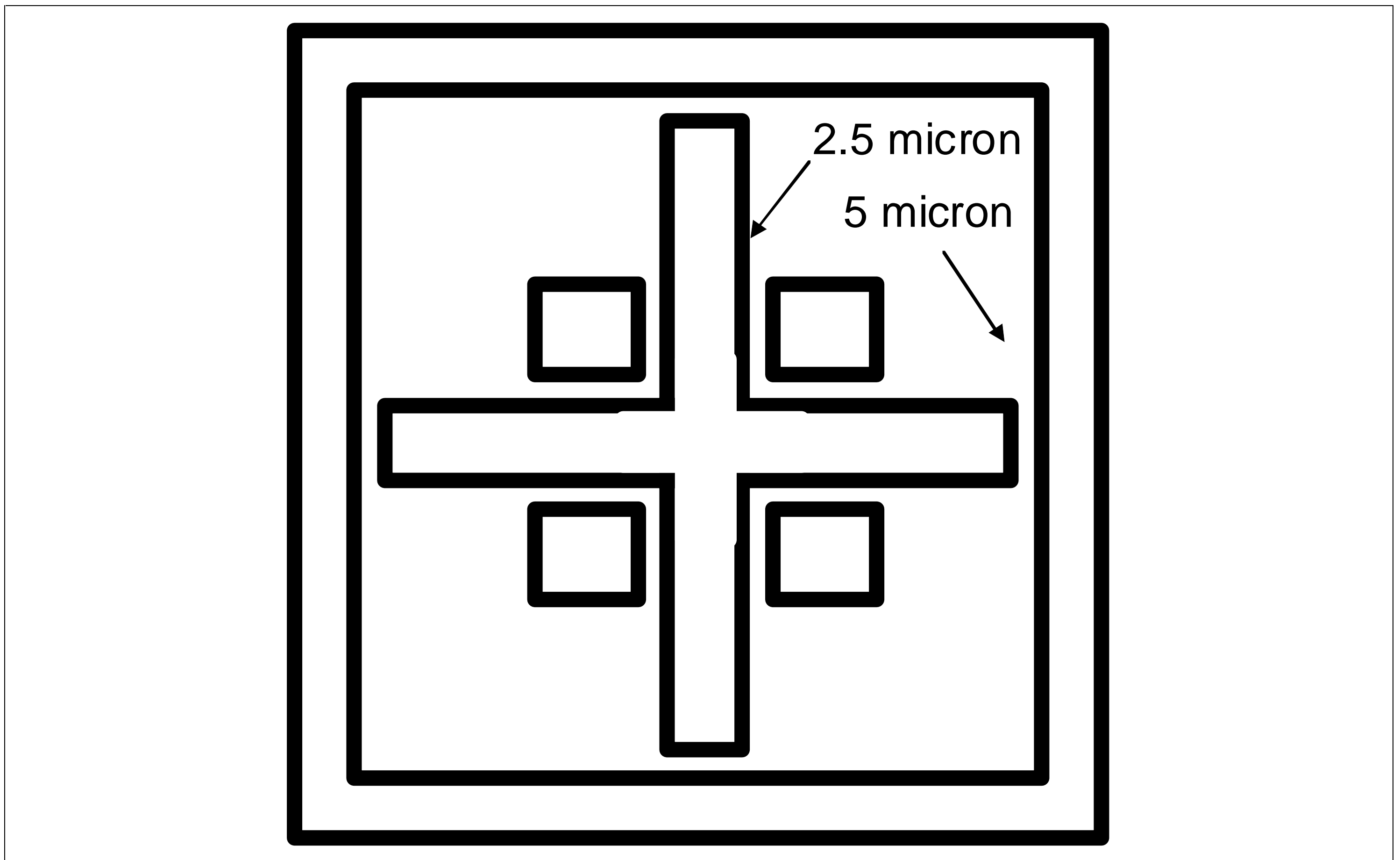
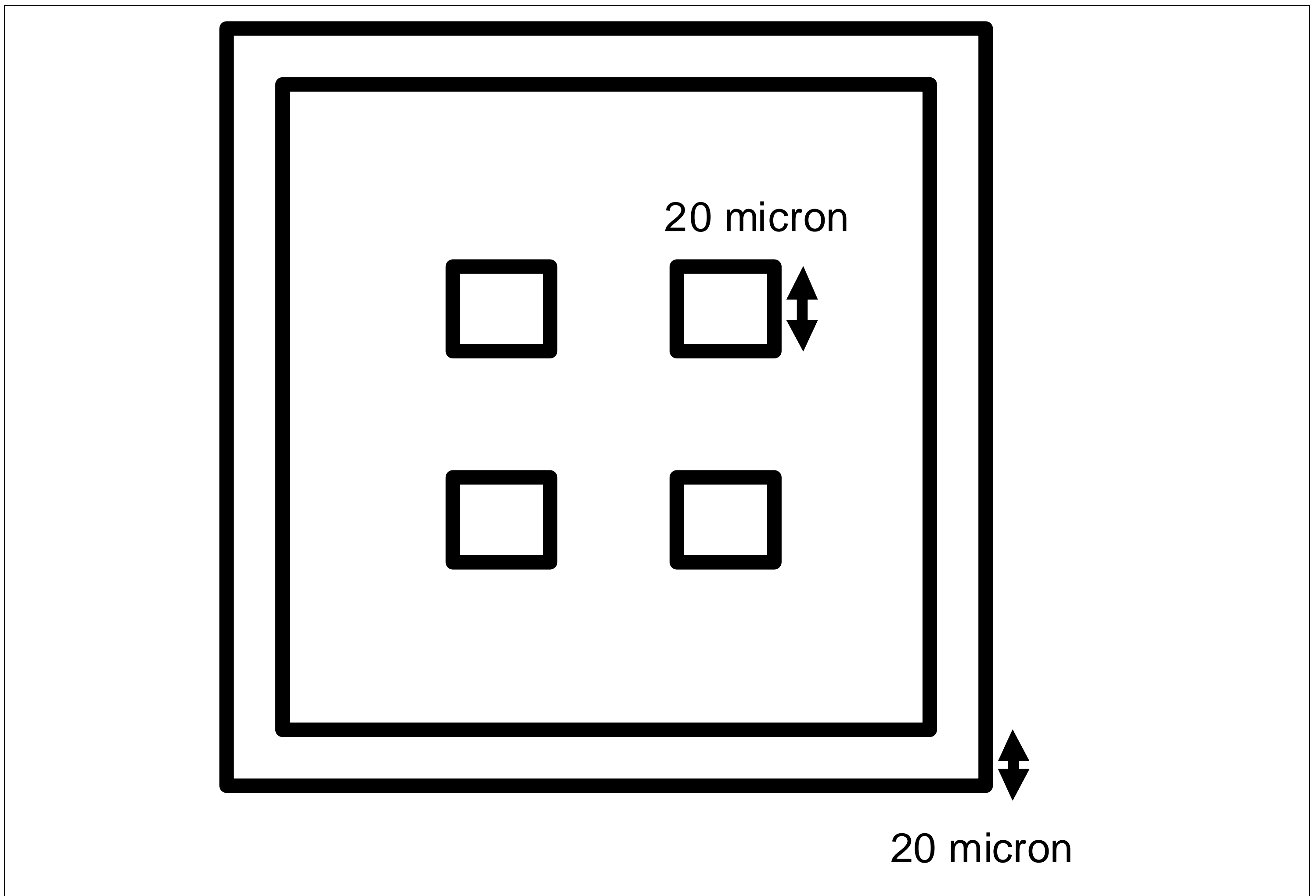
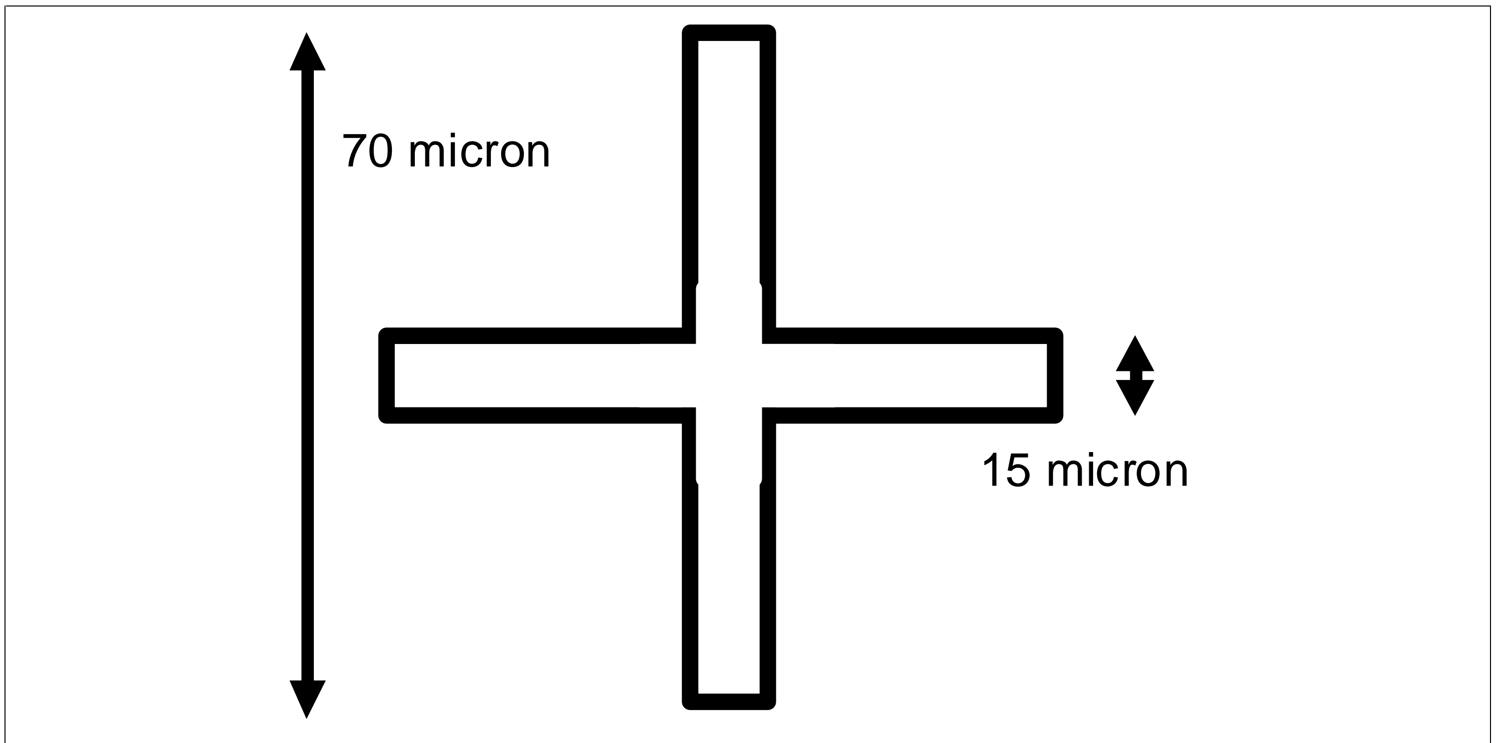
Shape (after alignment of pad or dielectric cut to first or last metal)



Shape (first or last metal)



Shape (pad or dielectric cut mask)



Minimum Separation from Port Area

100 microns

Support

Additional design support available from Ziptronix, Inc.

Category B – Copper to Copper Bonding (Tezzaron FaStack™)

This section describes the preferred surface configuration to facilitate mounting of the Intimate Memory onto any host device in a 3D configuration with FaStack Interconnect technology.

Form Factor

Semi-standard 200mm wafers. 300mm wafers can be accommodated by coring to 200mm.

Bow and Warp

Semi-standard

Back-End-of-Line (BEOL)

Aluminum or Copper (preferred)

Surface Configuration

1. Last bare metal after finishing
2. 100nm silicon oxide or oxy-nitride surface passivation after last metal finishing
3. Tezzaron tiled copper landing pad surface (preferred). Contact Tezzaron for additional information

Exposed electrical connections

Pads shall be:

15 x 15 um^2 Port Area centered within 25 x 25 um^2 cell.

Surface Planarity (Excluding Alignment Targets)

0.1 microns / 25 microns

1.0 microns or less total topography variation

Test Pads (Optional)

Test probe areas should be located remote to the active interconnect. Probe damage in the pad area can cause subsequent processing issues. Surface displacement after probing should be less than 1um.

Field Size

Maximum – 26mm x 31mm (X x Y)

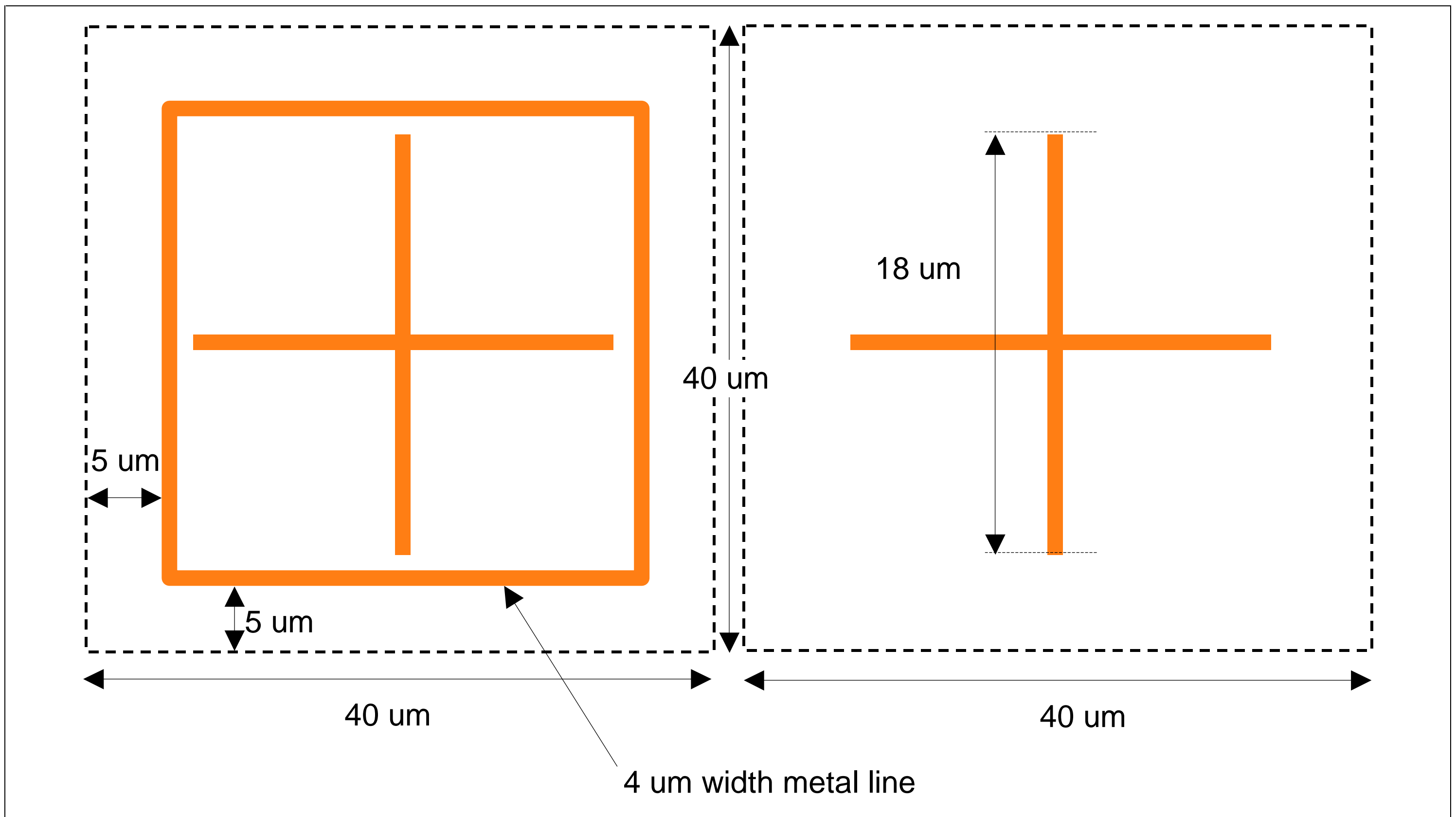
Alignment Targets

Targets for frontside pad metallization mask alignment:

1. Standard Nikon targets; Wx, Wy, LSAx, LSAy
2. Tezzaron copper land pattern already in place
3. The following is an alternative target set if one of the above 2 cases cannot be met.

Two targets are used and instantiated at least 4 times per wafer. Inclusion in the scribe area is good practice.

40 x 40 um Size, Overlay

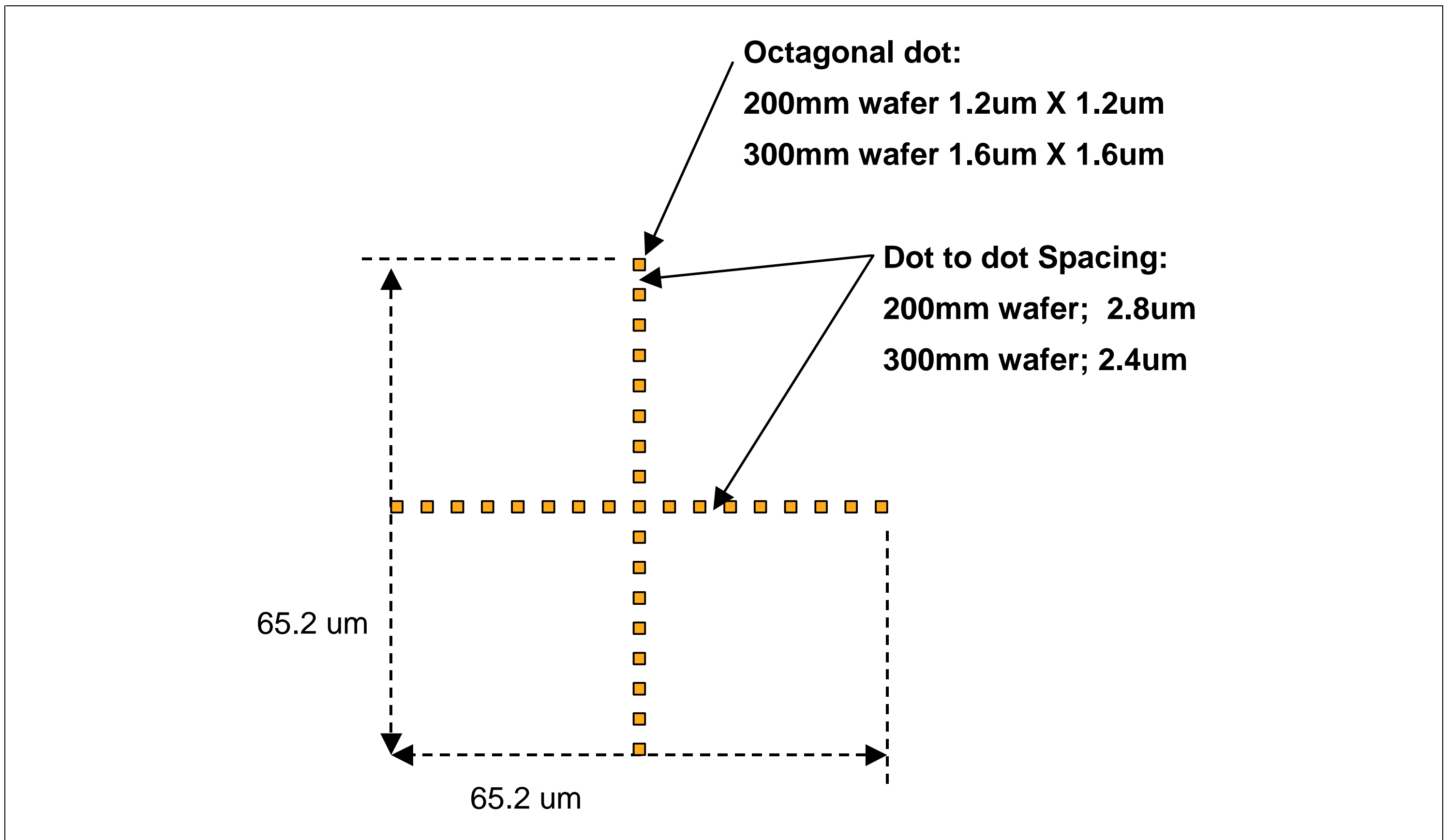


TSV targets for backside mask alignment:

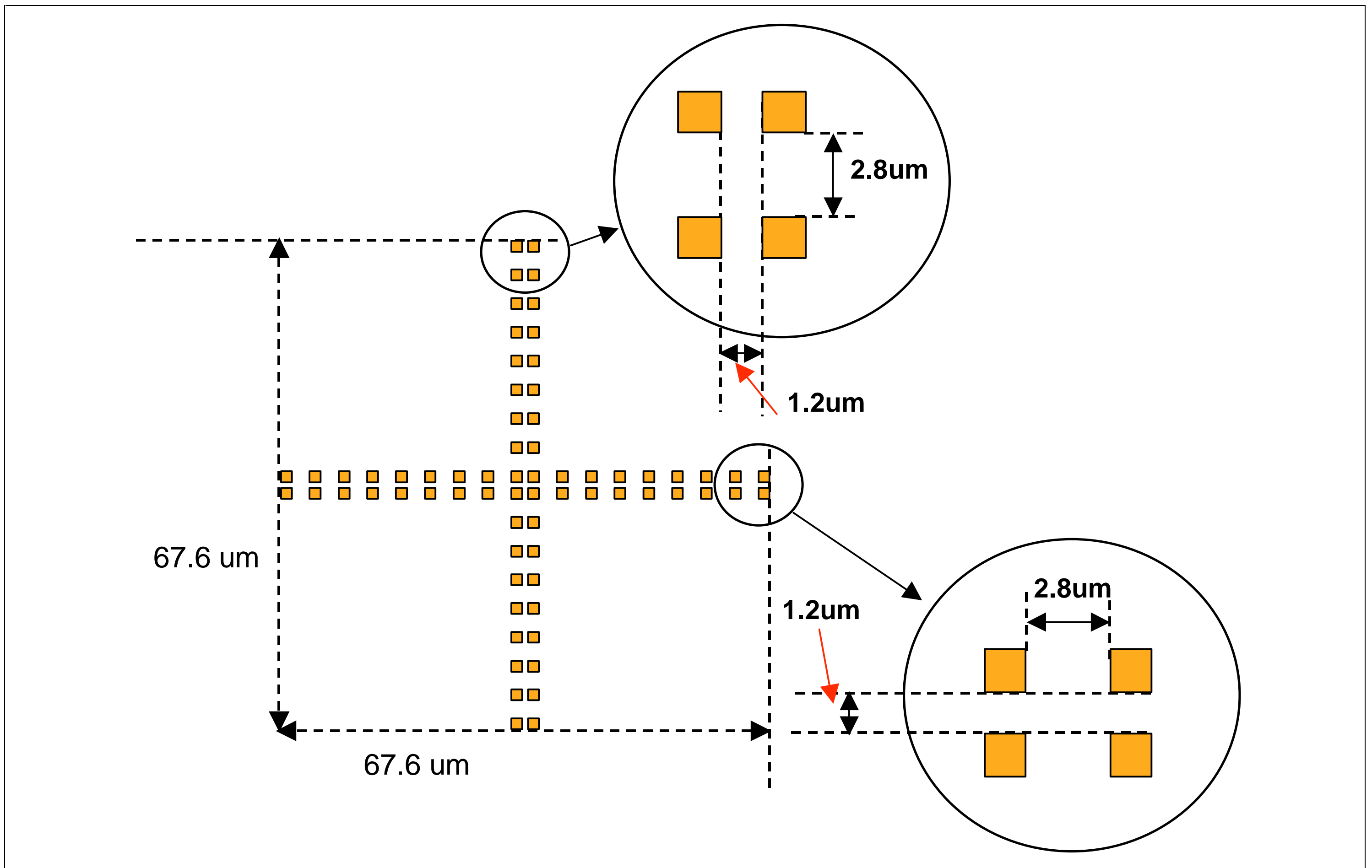
1. Standard Nikon targets; Wx, Wy, LSAx, LSAy
2. The following is an alternative target set if Nikon marks cannot be added.

Two targets are used and instantiated at least 4 times per wafer. Inclusion in the scribe area is good practice.

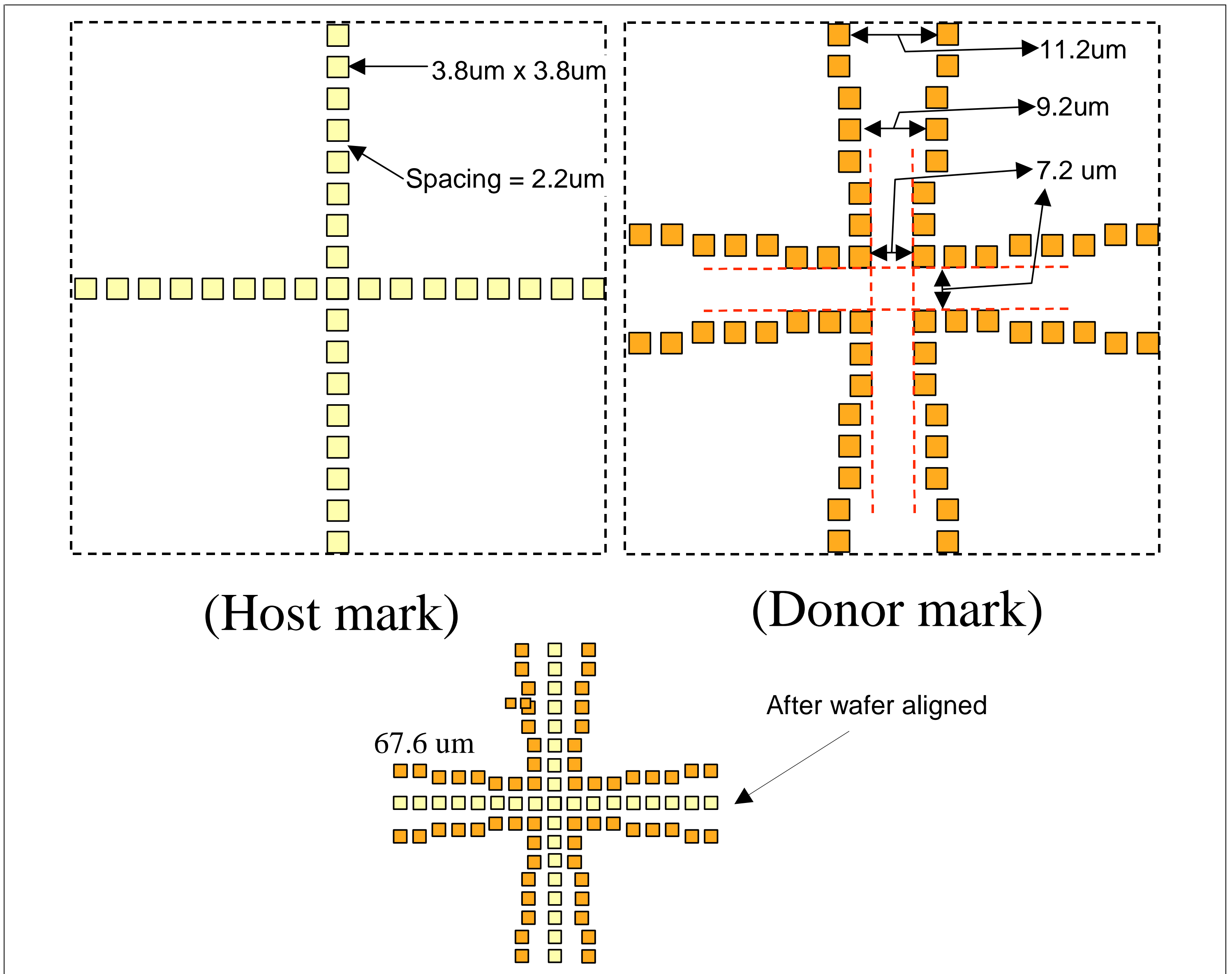
Backside alignment mark in TSV (i)



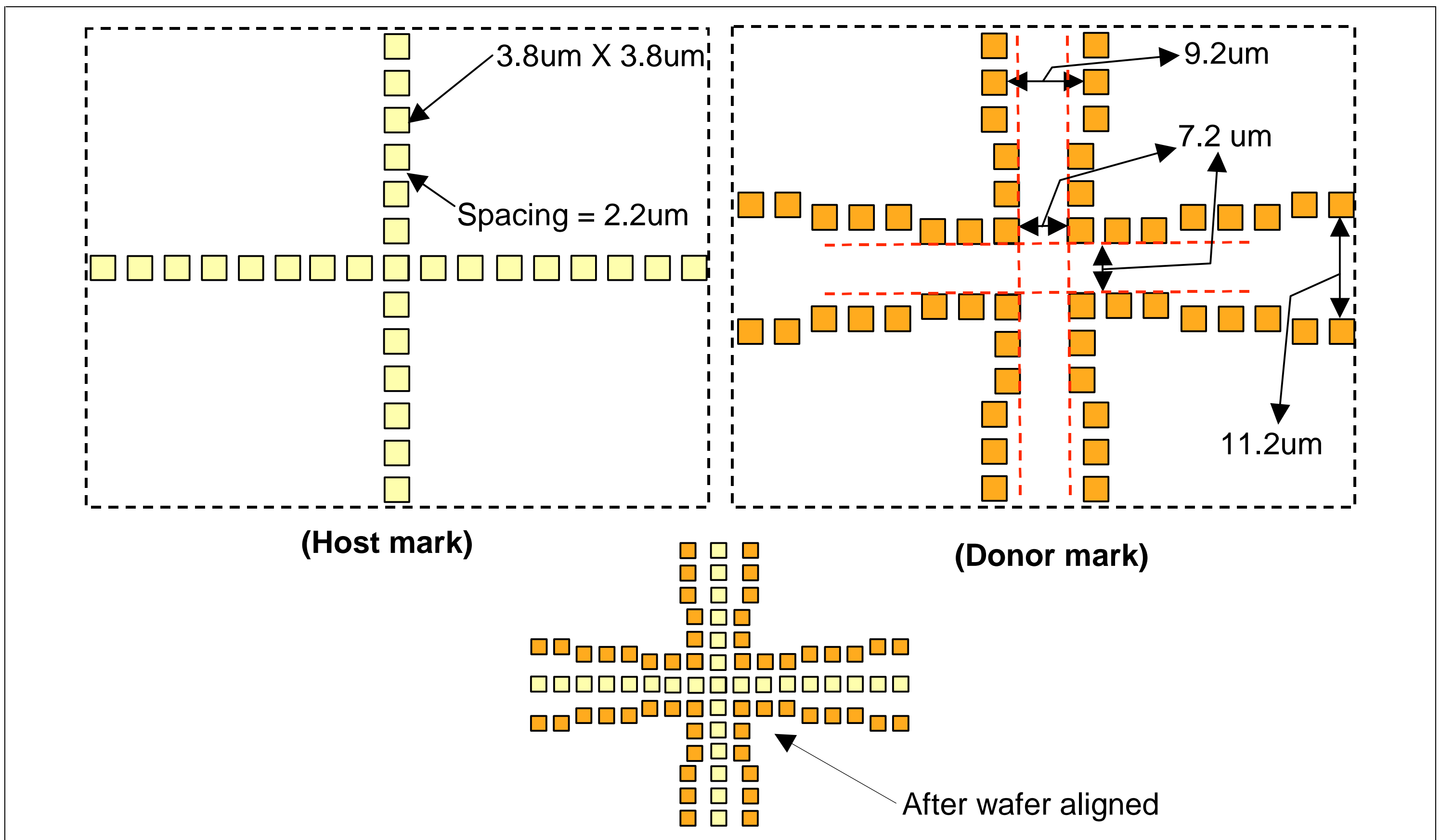
Backside alignment mark on pad reticle (ii)



IR alignment mark pair for wafer alignment (99.2 x 99.2 um)



IR alignment pair for wafer alignment: reduced height (99.2 x 75.2 um)
Two pairs of these marks should be used, with one rotated 90 degrees; one pair within each IR slit opening.



Topography

The wafer set must have the following alignment targets in top metal only. The targets must also be in clear field, (no metal including salicides or silicides):

The target keep away is 5um.

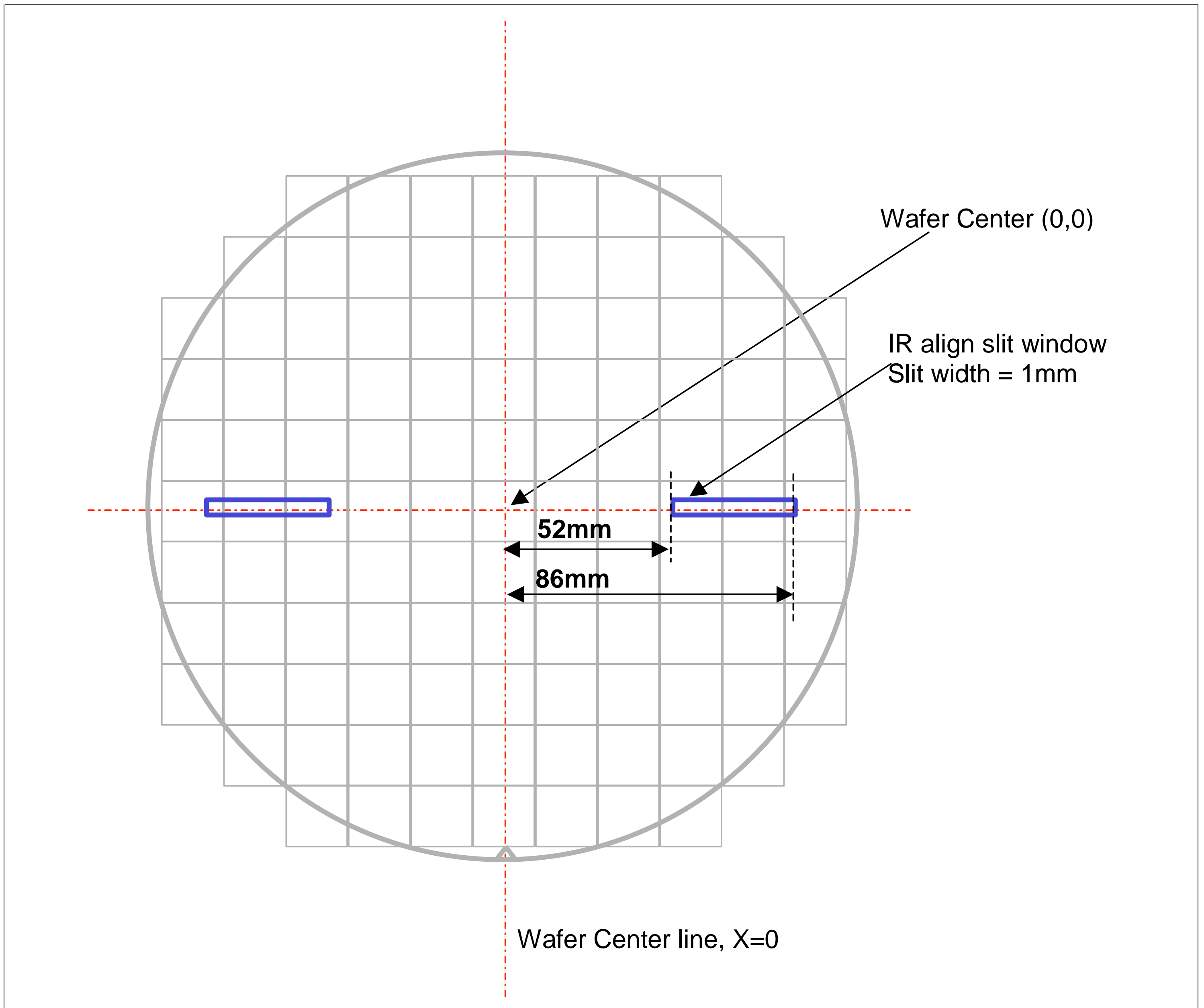
Number / area

1 per target area for 2 total targets

Location

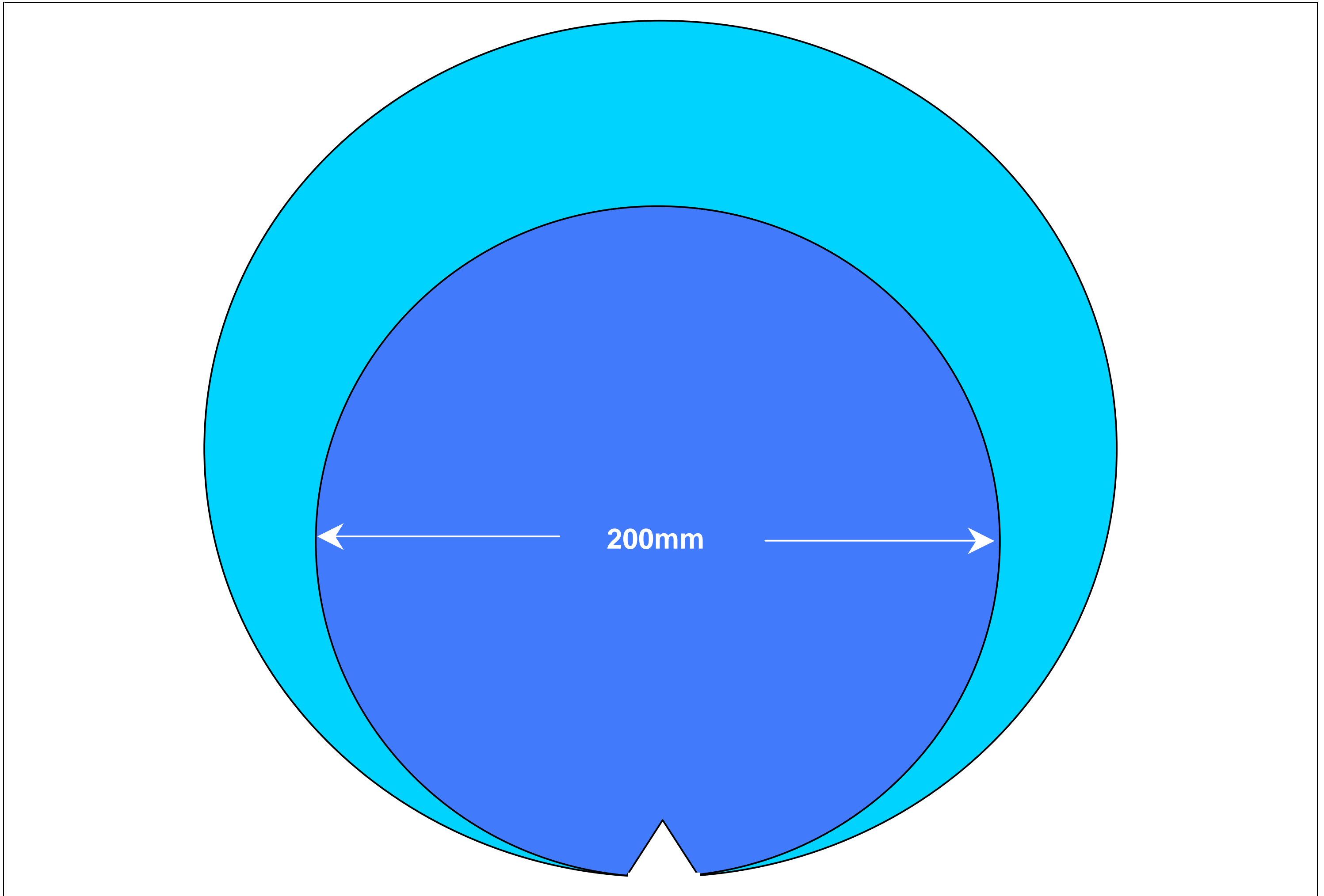
The targets must be within the following areas: The targets should be symmetric about the center.

200mm reference:



Above is the drawing for a 200mm. For cut down wafers, the same locations must be resultant after cut down. This puts the centerline at 100mm from the notch prior to cut down.

Cut down wafers must have notch and bevel. The original notch from the 300mm wafer is used for the resultant 200mm wafer.



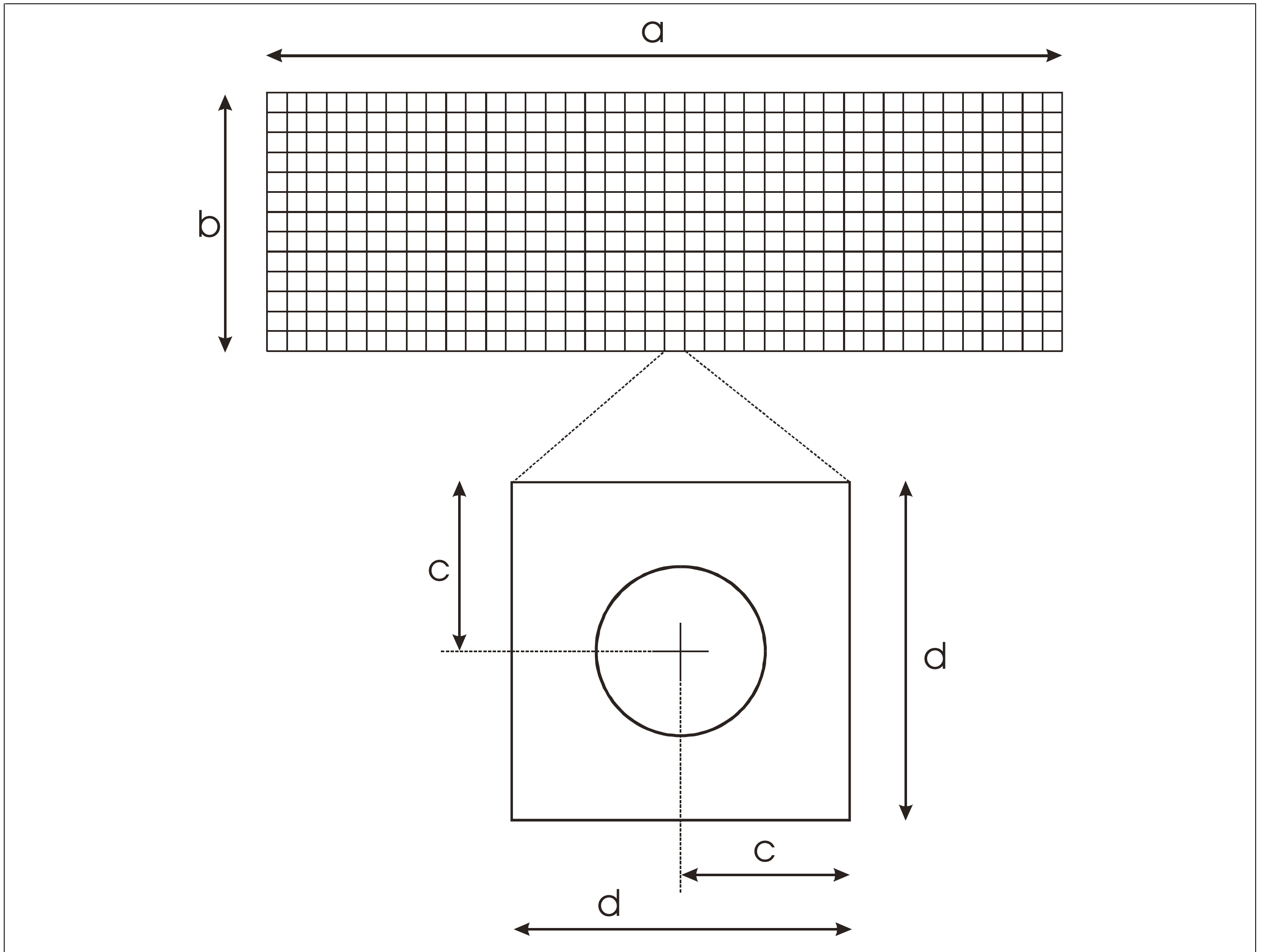
Support

Additional design support available from Tezzaron Semiconductor Corp.

Category C – (Reserved for future use)

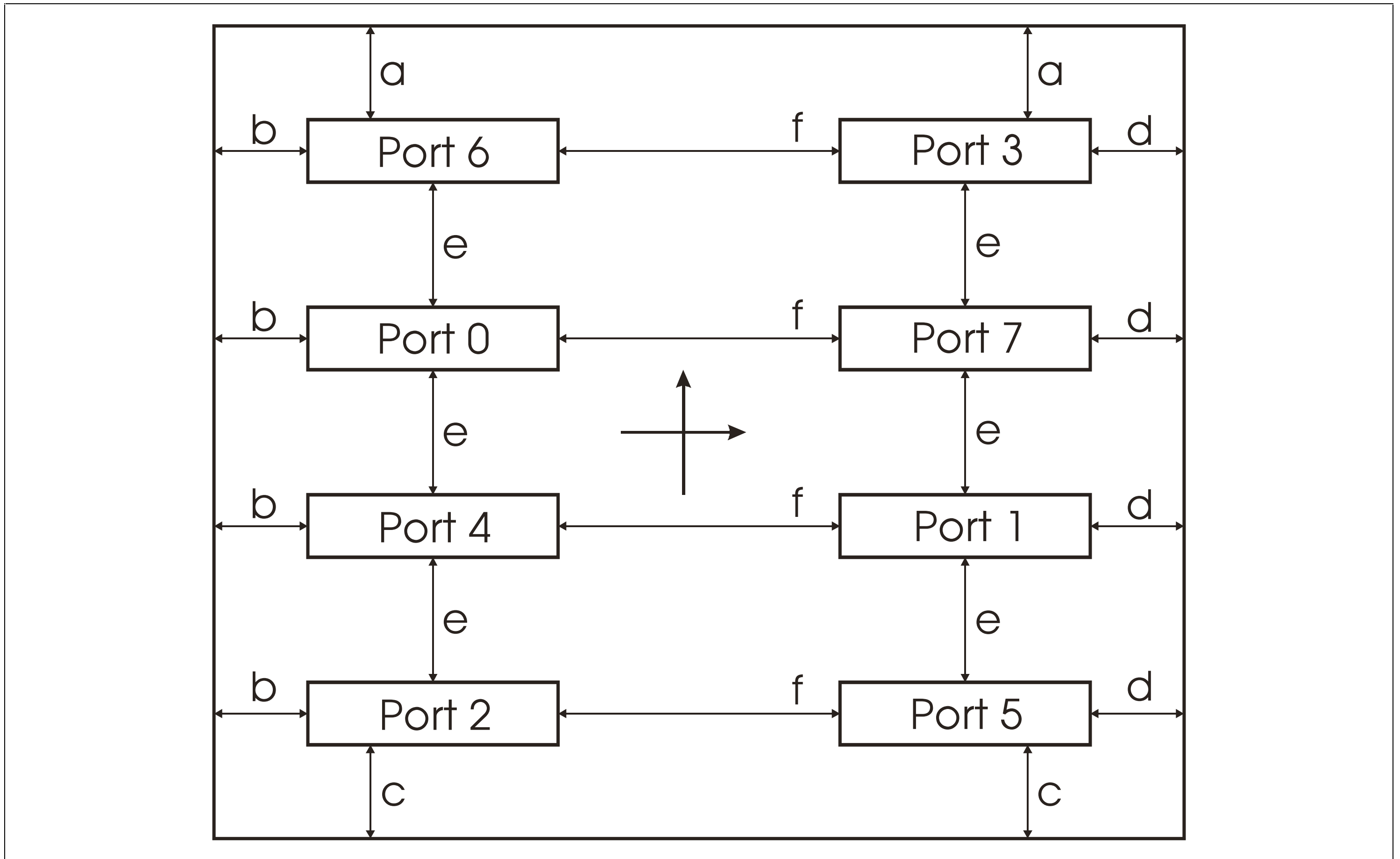
Footprint Diagrams

Port Layout (all variations)



Symbol	Description	Value
	Pad diameter/shape	per vendor
a	Port width	80 cells
b	Port height	19 cells
c	Center of pin to edge of cell	12.5μm
d	Edge of cell	25.0μm

Footprint Variation A



Symbol	Description	Value
	Port height	0.45mm
	Port width	2.00mm
a	Top margin	per vendor
b	Left margin	per vendor
c	Bottom margin	per vendor
d	Right margin	per vendor
e	Vertical port spacing	0.85mm
f	Horizontal port spacing	1.60mm