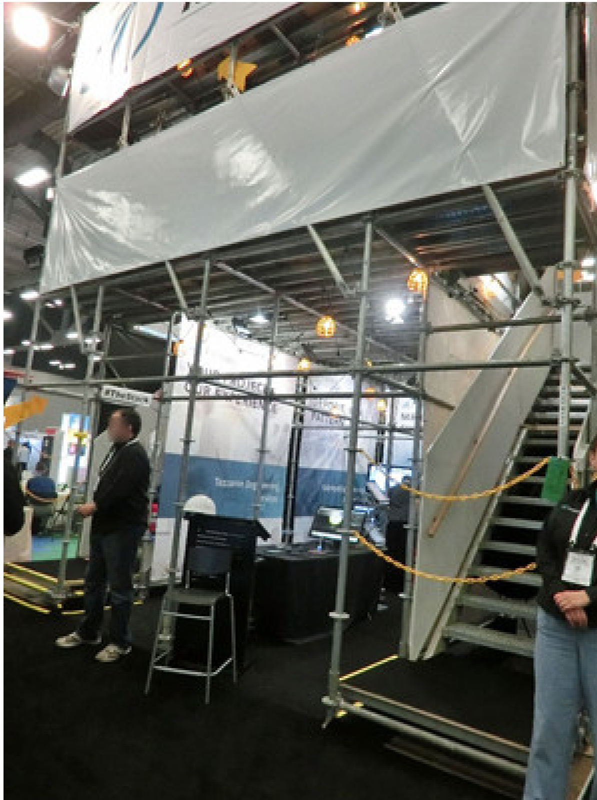
The following is a Google Translate version of:

http://news.mynavi.jp/articles/2016/01/06/sc15_tezzaron/

SC15 - Tezzaron maximum 18 DiRAM4 architecture of 3D implementation stacking wafers

- **HisA Ando [2016/01/06]**

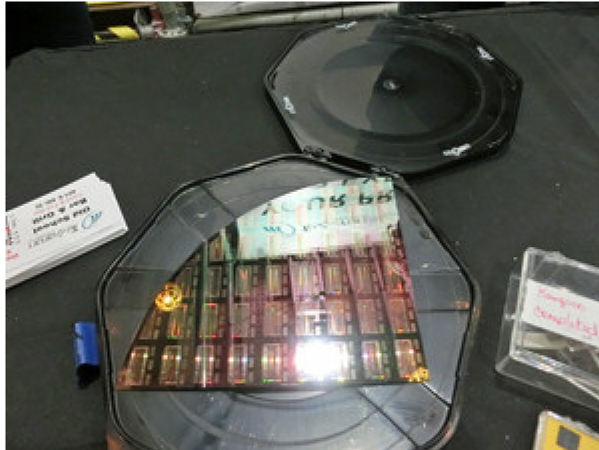
In exhibition hall of SC15, there was a iron pipe company that was making a tower of three floors in such as construction of scaffolding. In the company of "Tezzaron", and go up to the third floor, it was not when the entire exhibition hall overlooking attracting people through the front of the booth.



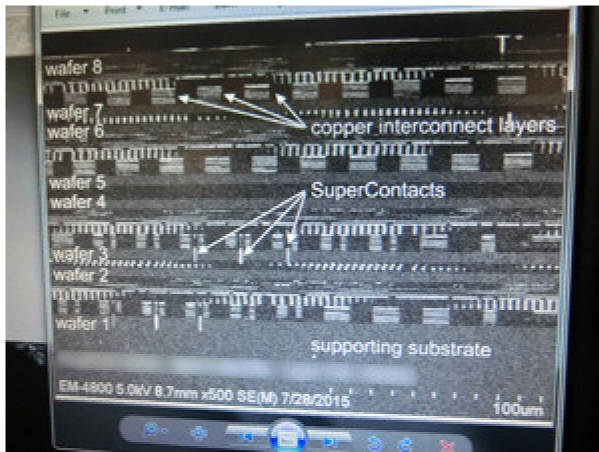
Tezzaron booth that had attracted the people by creating a three-story scaffolding

It is the thought or Abnormal, but was making things quite technically interesting. Although 3D implementation using TSV is a situation that is being put to practical use in the HBM and HMC, Tezzaron

of technology it is much higher density of connections than TSV, performance basis better that can make. It is another to a can be stacked up to 18 chips.



3D stacked wafer of Tezzaron. Which was cut to ¼



Wafer cross-sectional photograph of Tezzaron. This photo is 8 stacked

Point of stacking memory chips and control chips, as shown in the following figure, is similar to such HBM, a memory chip of the stack of Tezzaron is equipped with only the memory array, peripheral circuits of the memory such as decoders or sense amplifiers it is placed in the control chip. This way to reduce the memory chip in that it does not contain a peripheral circuit, or it can be packed more bits in the memory chip.

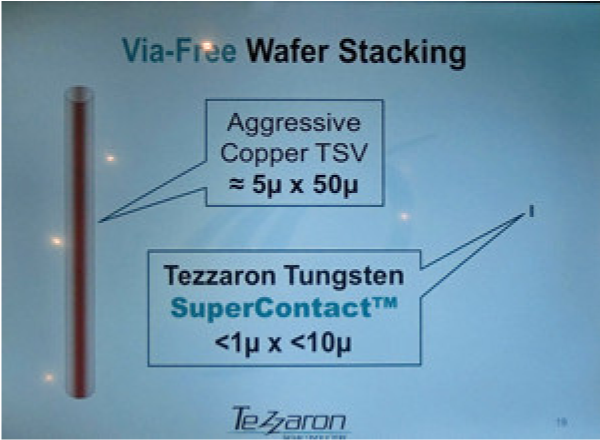
When the peripheral circuit to another chip, in general, or increasing the number of connections and memory chips, but a problem that the wiring may become long out, the connection between the Tezzaron of the chip is much smaller than the TSV, connections in the chip and remainder and

unchanged, that does not become a problem. Since making the RAM in a form that is degraded in this way for each element, Tezzaron can mean that Dis Integrated a RAM, is called "DiRAM4 Architecture".

16 pieces of memory chips and control layer, examples of stacking chips of the I/O layer

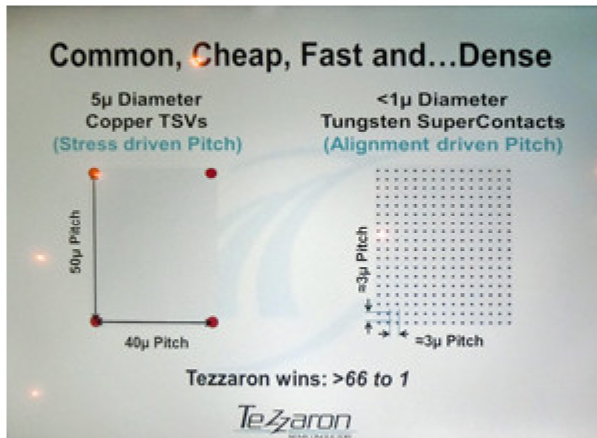
Normal TSV, the use of copper in connection passing through the wafer, be those aggressive, it is 5µm, is about 50µm length diameter. This for the connection of Tezzaron uses tungsten, it is following in the even 10µm or less and a short length 1µm diameter.

Connection with tungsten is widely used to connect the metal wiring of a MOS transistor and a first layer made of the silicon layer of the LSI chip, it is an established technique can fine connections. However, it cannot be only 10µm or less (story about 6µm be heard) of the connection, it is necessary to make the wafer less the thickness of.



Connection of Tezzaron diameter 1µm or less, following a small 10µm length

Viewed in a plane direction, and is usually of one for the area of the TSV at 40µm × 50µm connection, or one and 200 times the 3µm × 3µm in manner Tezzaron (and is written 66 times in the figure) I can of the density connection. For TSV by leaving a large hole in the wafer determine the mechanical stress the pitch by making TSV, but the method of Tezzaron not stress that is predetermined pitch in the alignment accuracy.



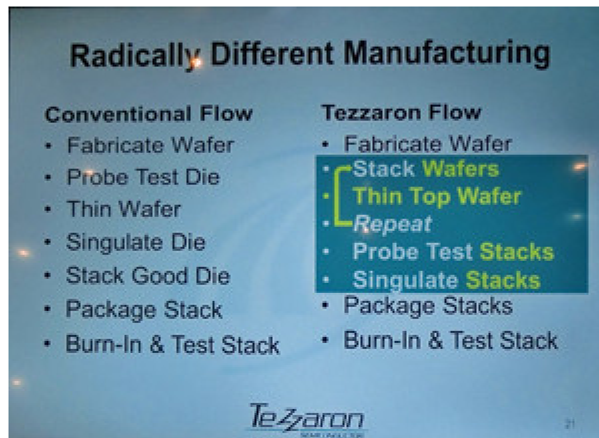
Connecting Tezzaron, compared to normal TSV, may overwhelmingly high density connections

For regular TSV, to produce the wafers were examined in a probe test, and put to remember the position of the non-defective chip. Then, by polishing to a thickness of the wafer of about 50µm, and the chips by cutting it. It was placed in a package by performing lamination by selecting non-defective chips, and are manufactured by the procedure of performing the burn-in and testing.

To achieve a thin wafer of 10µm or less, in the case of Tezzaron, and starting from a certain degree of thickness of the base wafer (Supporting Substrate), and when performing the joining of the next wafer, the steps of polishing thin top wafer repeat. In this way, the subject to be polished becomes thicker than the base wafer, need no longer that polishing the fragile wafer of ultrathin of 10µm or less. However, each one wafer stack, it is necessary to repeat the grinding.

Note that without such a solder in the joint, and that is joined on heating to suit the position of about 200 °C.

Then, when finished stack of required number of wafers to be subjected to a probe test is placed in a package by selecting a stack of non-defective by cutting the wafer, to perform burn-in and testing.

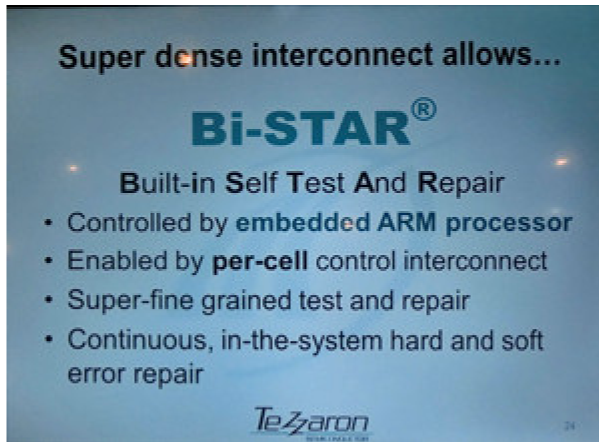


Tezzaron is, cannot be tested until the end of the stacking of all of the wafer

In the TSV process, the memory wafers are inspected one by one, the bad chip at the stage of making the final stack is removed from the stack assembly. However, in the case of Tezzaron, it is not possible to test in diameter 1µm electrode for connecting the memory wafers too small by contacting a probe. Further, since the bonding wafers to each other, it is impossible to exclude them even if defective chip.

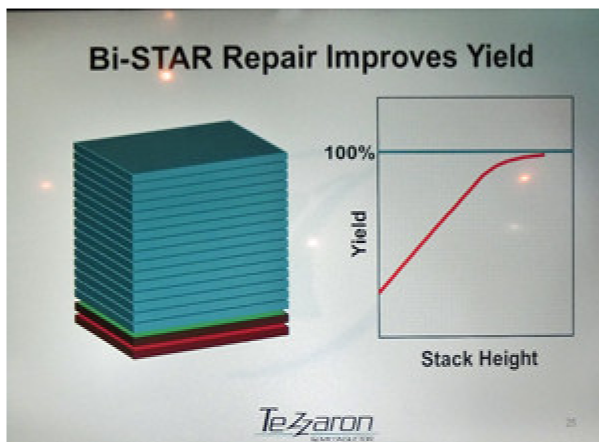
Therefore, such in the way the yield of the stack of non-defective product is very low, because practical use must not was a general view.

Tezzaron devised a way of "BiSTAR (Built in Self -test and Repair)" On the contrary. BiSTAR utilizes a can be performed by connecting a short high density connections between wafer and separating the sub-array with defective in memory chips, replaced by sub-array of non-defective. This is replaced circuit is put in a state of being incorporated in a pre-chip.



It was tested in a state in which the entire wafer is laminated to repair except for the defective part BiSTAR

The connection between the wafers is short, the spare sub-array need not be in the same chip, it may be in another wafer. Therefore, the number of wafers to stack also increases the number of spare sub-array according to the increase, as shown in the following figure, that the probability of a stack of non-defective product can be obtained increases as the number of wafers of the stack increases.



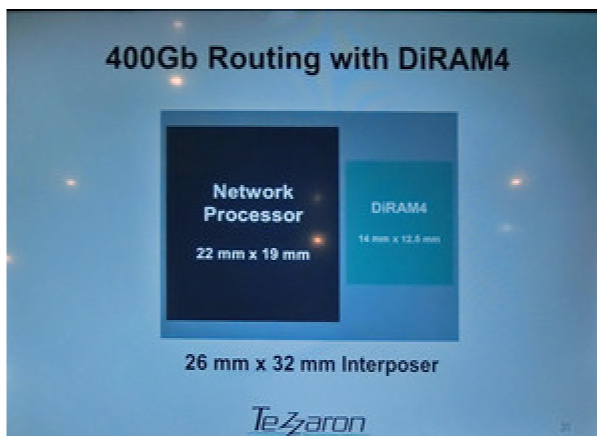
When the number of sheets of the stack to the wafer increases, so increases also the number of spare sub-array, the yield that uses a BiSTAR repair to improve

1 thinning of the wafer by the polishing and the bonding of each wafer of Tezzaron is, certainly, but the manufacturing process is complicated becomes a factor of cost, this technology is a high density of connection can be realized more than 100 times as compared to the TSV connection The use if, and as a high-density memory to the extent that cannot be realized and without a 10nm technology can be implemented in a 45nm technology. Therefore, even if the assembly process becomes cost to some

extent, since products that are differentiated in terms of memory capacity it makes, as a whole is advantageous.

In addition, there is an advantage due to the fact that performance is improved. Network processor requires a high-speed memory access, in order to perform the processing for packet communication 400Gbit / s requires access 1TB / s in the DRAM 4Gbit the packet buffer, and a table access 12BT / s at 576Mbit, 576Mbit/s in that there is a need for SigmaQuad-IIIe memory that can access the 5TB/s.

To do this requires a thirty DDR3 DRAM and 12 of RLDRAM3 chips and four SRAM, but if you use a 3D stacked DiRAM4 of Tezzaron is to be satisfied by a single stack, is resting on the interposer of 26mm × 32mm to become. Therefore, the entire apparatus, cost reduction can be achieved over the cost of the 3D stack of Tezzaron.



But when the network processor of memory to perform the routing of 400Gb/ s made using a commercially available memory chip 50 near the memory chips is a must, if you use the DiRAM4 of Tezzaron can be realized in one stack, the interposer of 26mm × 32mm I would ride