DiRAM™ Architecture Makes Disintegration a Good Thing

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Old News

- Conventional Si approaches are failing
  - Performance is too low
  - Power is too high
- 2.5D and 3D hold great promise
  - Costs look problematic
  - Performance improvements marginal
  - Power is *still* too high

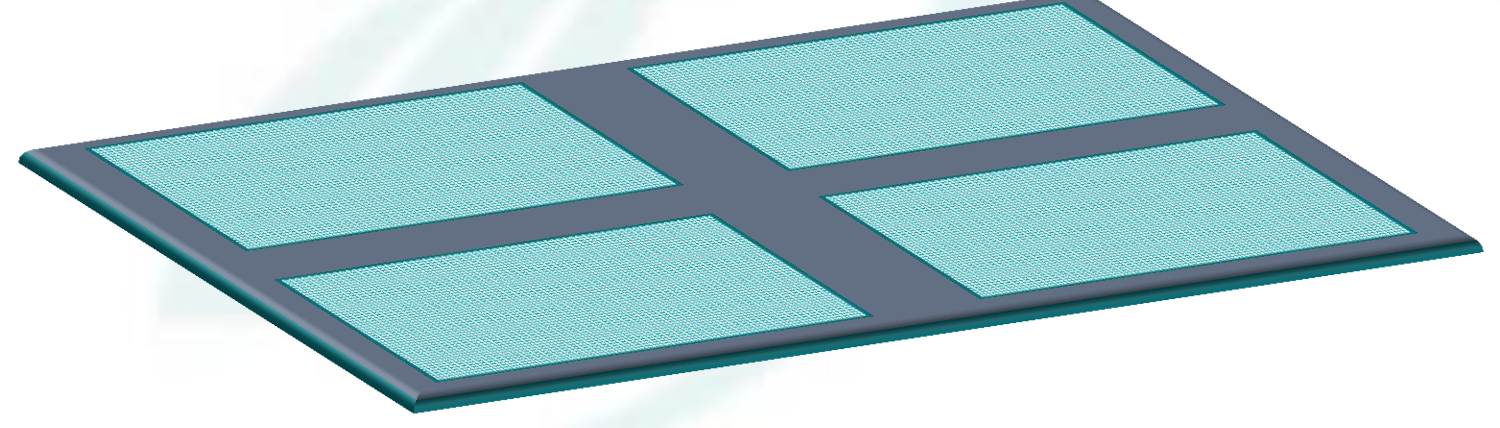
Step 1: Set A Huge Goal

- **64 Gb** of RAM in 175 mm^2
- **256** fully independent Channels
- **16 Banks** per Channel
- **64 bit** Sep I/O Data per Channel
- **12ns tRC** (RAS to RAS in a Bank)
- **16 Tb/s Data Bandwidth**
- Competitive Manufacturing Cost

Conventional RAM

With Conventional RAM design and packaging?

Impossible



Stack Conventional RAM

With Conventional RAM design and 3D packaging?

Still impossible

Sliced 3D RAM Architecture

With Sliced 3D RAM design and 3D packaging?

Still impossible

Step 2: Take an Audacious Approach

Dis-Integrated 3D RAM

VERY Possible

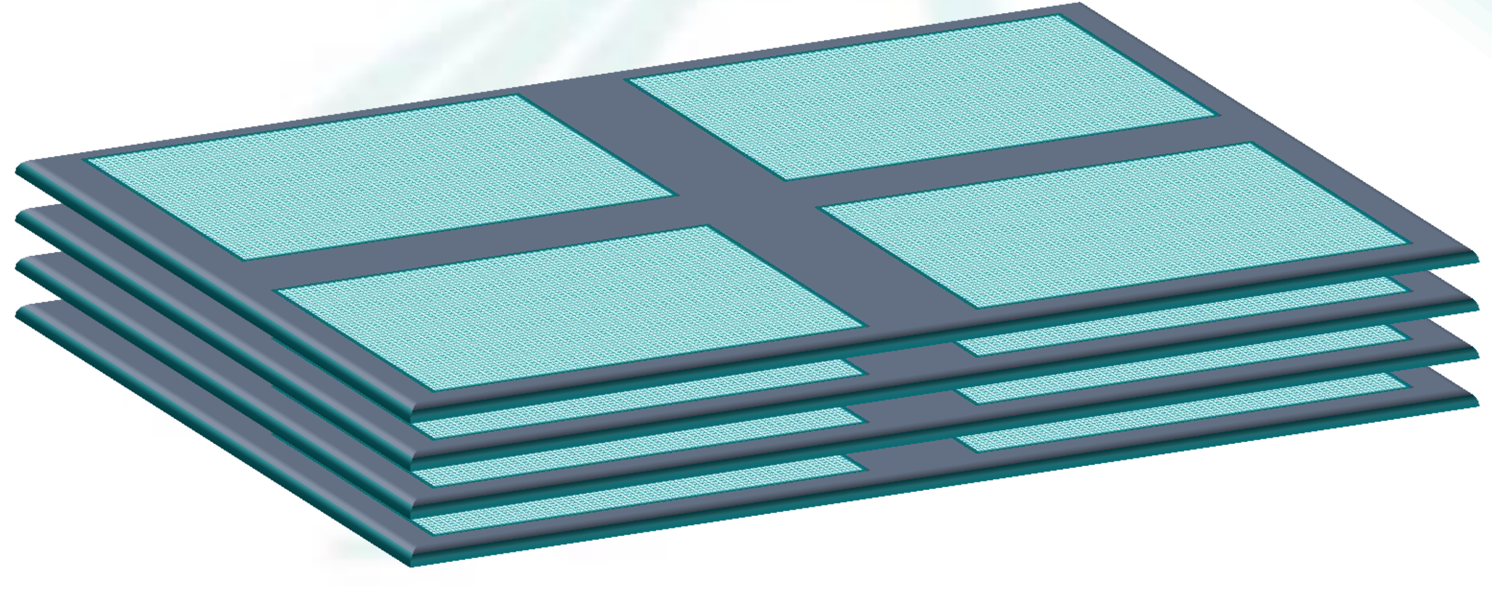
Conventional RAM Architecture

Memory Bits

Periphery
- Decoders
- Amps
- Drivers
- etc.

Conventional 3D *Packaging*

- Preserves traditional RAM problems
- Adds stacking costs



Sliced 3D RAM Architecture

Memory Bits

Periphery

- Decoders
- Amps
- Drivers
- etc.

DiRAM™ True 3D RAM Architecture

I/O Layer

Dis-Integrated 3D RAM Architecture

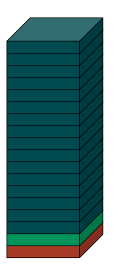
DiRAM™ Architecture

Memory Cells
and
Access Transistors

Sense Amps, etc.

I/O Layer

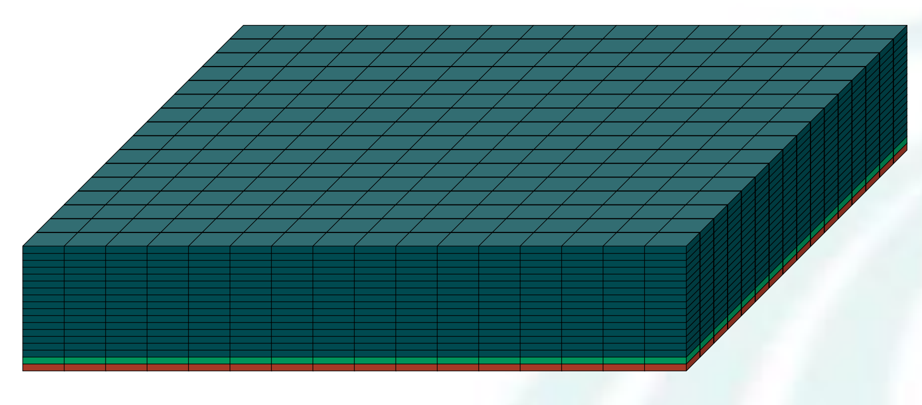
256 Independent Channels



Each Channel

- 256 Mb Storage
- 64 Gb/s Bandwidth
- 7ns RAS Latency
- 12ns tRC
- 16 Paired Banks
- 83 MT/s Transaction Rate

DiRAM4 Stack Performance



256 Independent Channels

- **64** Gb Storage
- **16.4** Terabit/s Data Bandwidth
- **4096** Banks
- **21** Billion Transactions Per Second (Minimum)

DiRAM4 Scale* Drawing

14 mm

Top View

175 mm²

12.5 mm

Side View

0.5 mm

87.5 mm³

Isometric View

* Almost to scale

Via-Free Wafer Stacking

Aggressive
Copper TSV
≈ 10μ x 50μ

2x

Tezzaron Tungsten
SuperContact™
≈ 1μ x 5.5μ

SuperContacts™

- **Easier/cheaper to manufacture**
  - Tungsten not Copper
- **Electrically superior**
  - Less parasitic loading
- **Smaller diameter**
  - MUCH higher interconnect density

Radically Different Manufacturing

Conventional Flow

- Fabricate Wafer
- Probe Test Die
- Thin Wafer
- Singulate Die
- Stack Good Die
- Package Stack
- Burn-In & Test Stack

Tezzaron Flow

- Fabricate Wafer
- **Stack Wafers**
- **Thin Top Wafer**
- ***Repeat***
- **Probe Test Stacks**
- **Singulate Stacks**
- Package Stacks
- Burn-In & Test Stack

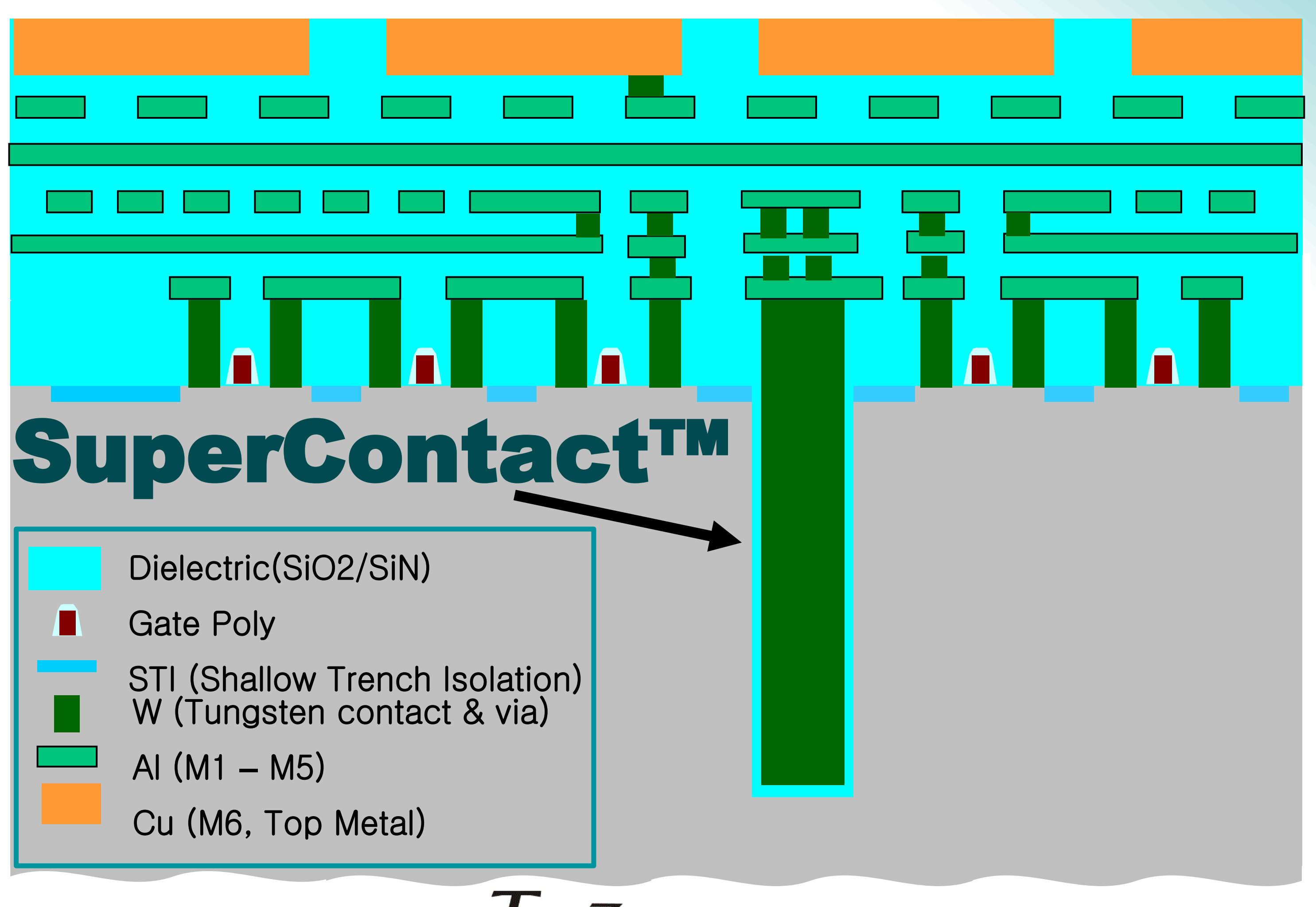
<u>Never</u> Handle A Thin Wafer

<u>The Tezzaron Mantra</u>

Bond Two…Grind One

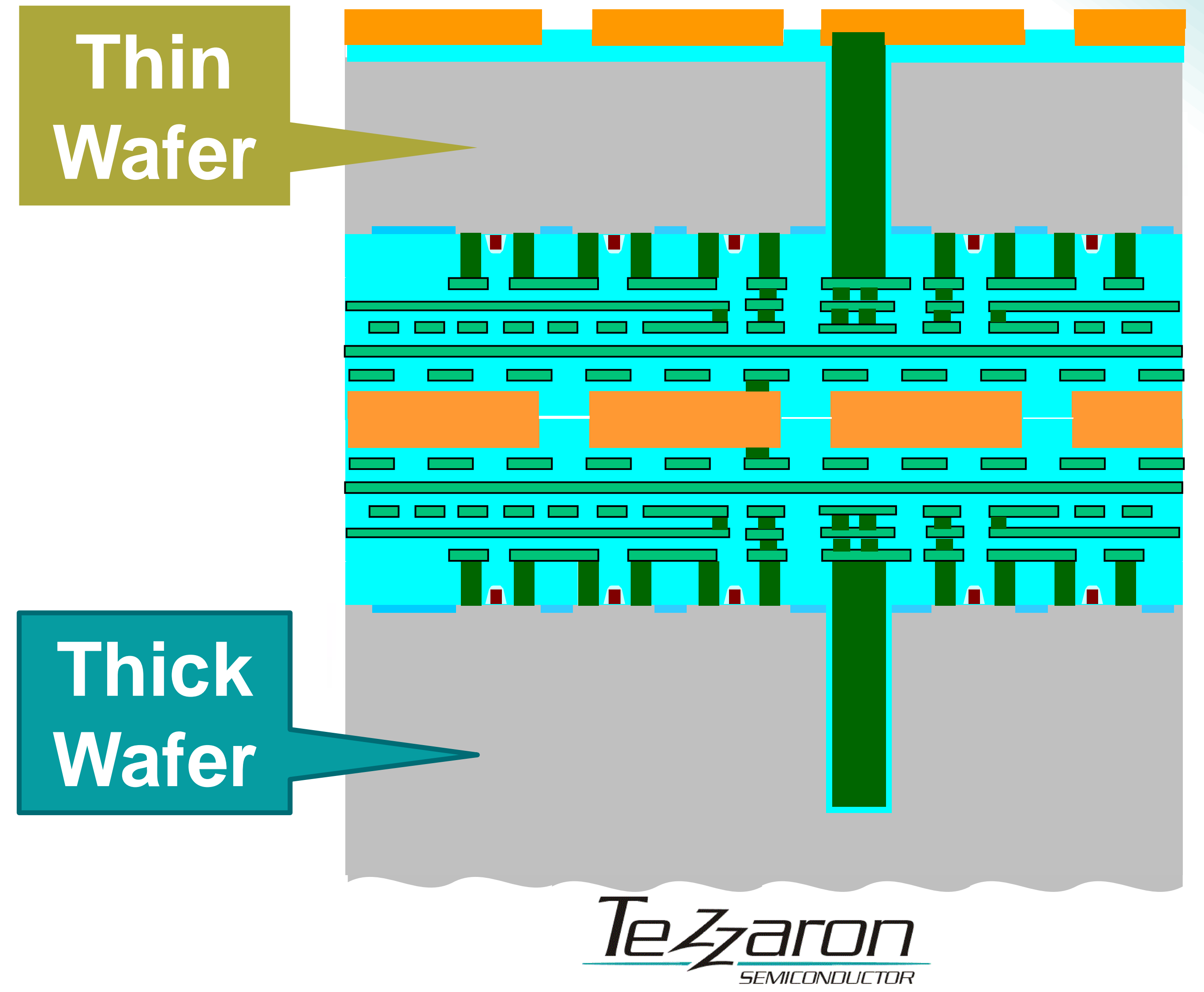
…to make the world's thinnest RAM wafers

Step 1 – Build, Drill, Fill & Metalize



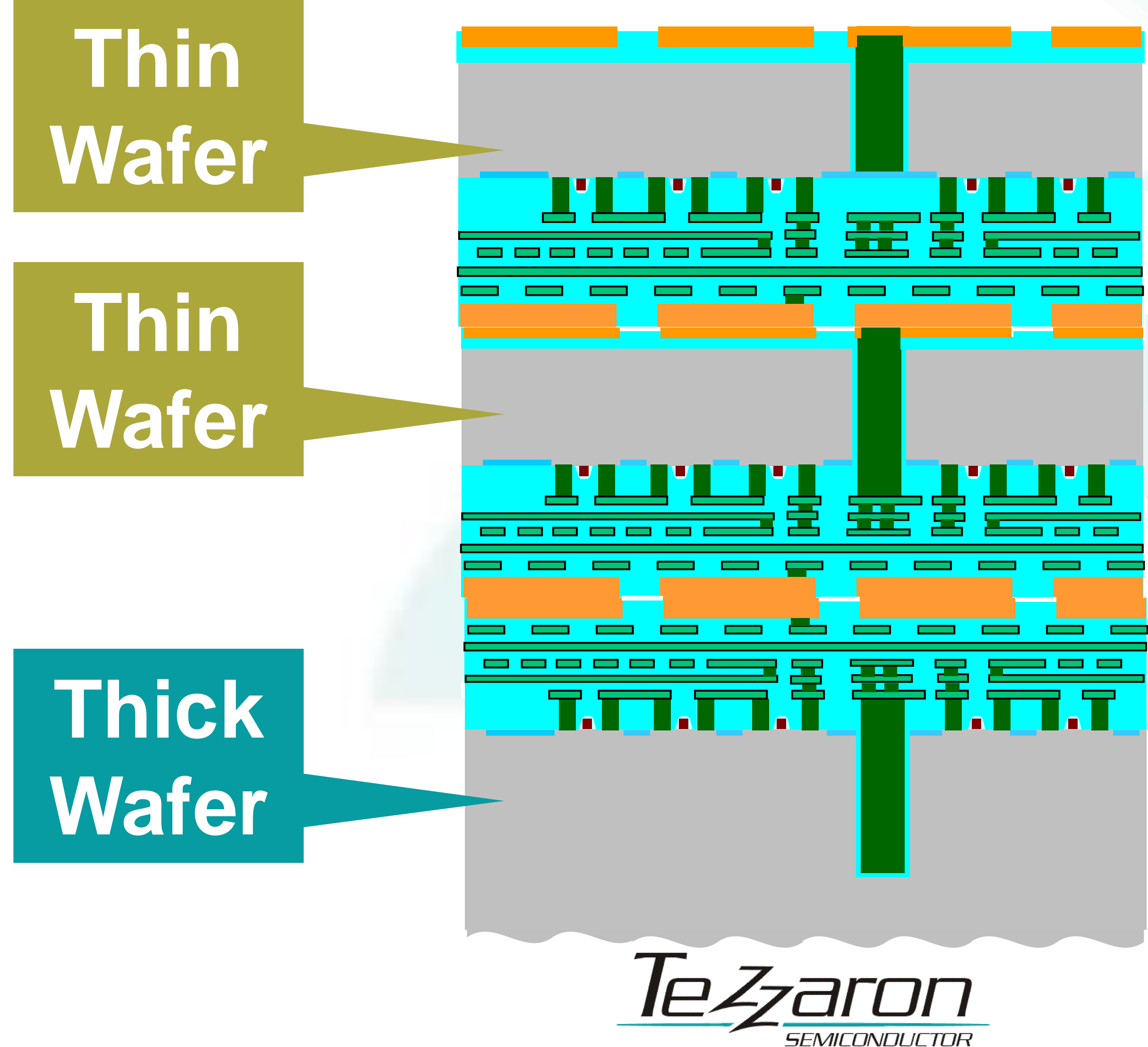
Tezzaron SEMICONDUCTOR

Step 2 – Bond, Thin & Re-metal



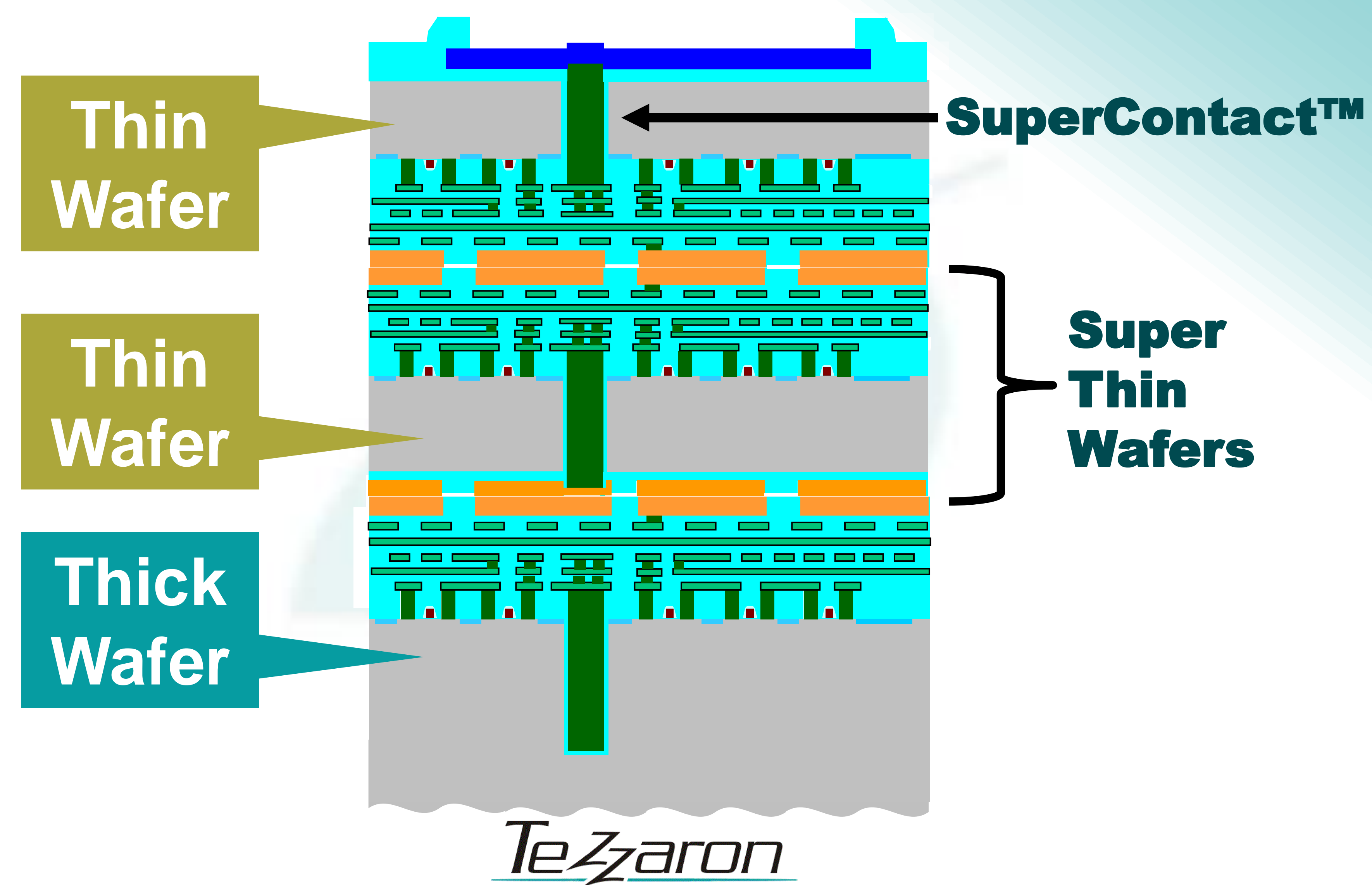
Tezzaron SEMICONDUCTOR

Step (n-1) – Rinse and Repeat



Tezzaron SEMICONDUCTOR

Step n – Build I/O Pads



"That can't work…"

"…bonding un-tested die will produce **near zero yields**, **poor reliability** and **high costs**."

Translation

You Tezzaron people are crazy!

Novati Technologies - Austin

- Tezzaron subsidiary
  - Manufacturing volume
  - Services available
- 3D Assembly Options
  - Cu-Cu
  - DBI®,
  - Oxide Bonding
  - Intermetallic
  - Gold-Indium, Gold-Gold
- Silicon Interposers
  - Passive
  - Passive Plus
  - Active

Super dense interconnect allows…

Bi-STAR™

Built-**i**n **S**elf **T**est **A**nd **R**epair

- Controlled by **embedded ARM processor**
- Enabled by **per-cell** control interconnect
- Super-fine grained test and repair
- Continuous, in-the-system hard and soft error repair

Bi-STAR™ Does More, Works Better

Bi-STAR Repairs

- Bad memory cells
- Bad line drivers
- Bad sense amps
- Shorted word lines
- Shorted bit-lines
- Leaky bits
- Bad secondary bus drivers

Bi-STAR Tests

- Tests > 300,000 nodes per clock cycle
- Tests > 1,000x faster than external memory tester
- Via SPI port, works with Host to allow continuous scrub / repair

Bi-STAR Repair Improves Yield

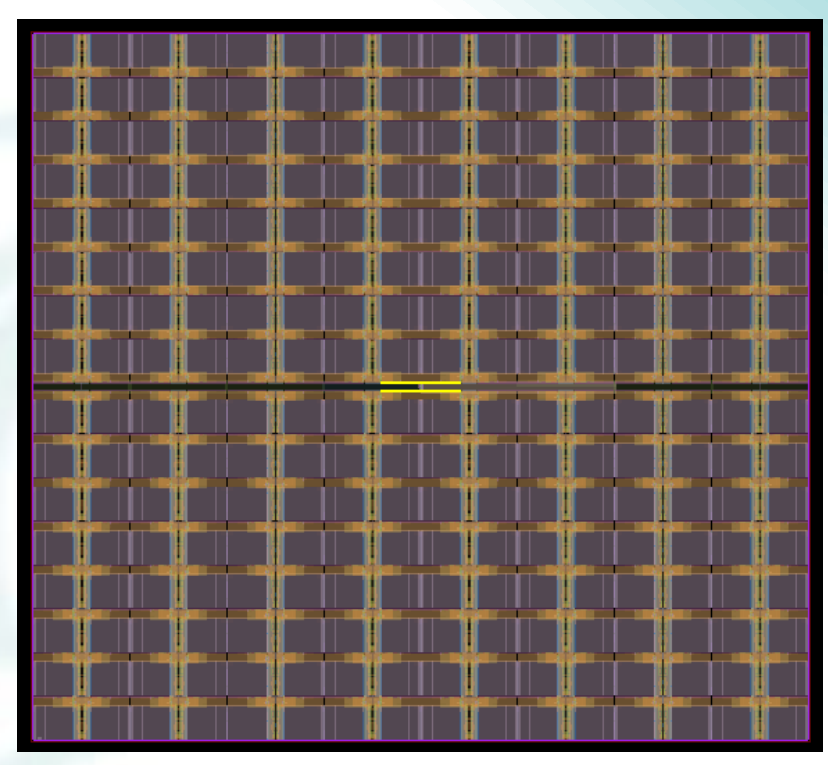
100%

Yield

Stack Height

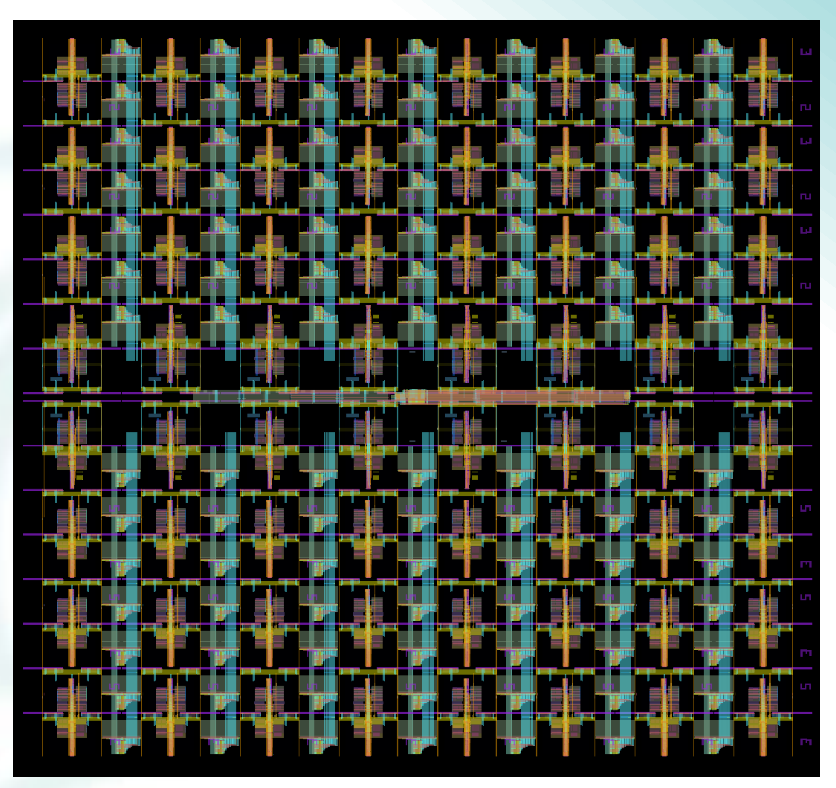
DiRAM4 Controller Layer

- GF 40nm LP
  - 300mm, 8 M, 1P
- Content
  - Sense Amps
  - Word Line Decoders
  - **Mapping CAMS**
  - **ECC Ckts & Test Sequencers**
- Bonding
  - Front-to-Front of Bits
  - Back-to-Front of I/O



DiRAM4 2.5D I/O Layer

- GF 65nm LPE
  - 300mm, 8 M, 1 P
- Content
  - I/O Buffers
  - **ARM M0+ Core**
  - **12Kb eFuse Block**
  - 24Mb SRAM
  - 8Mb ROM
  - SPI Serial Port
- Bonding
  - Front-to-Back of Contl
  - Back to C4 Balls
    - 184μ x 70μm pitch



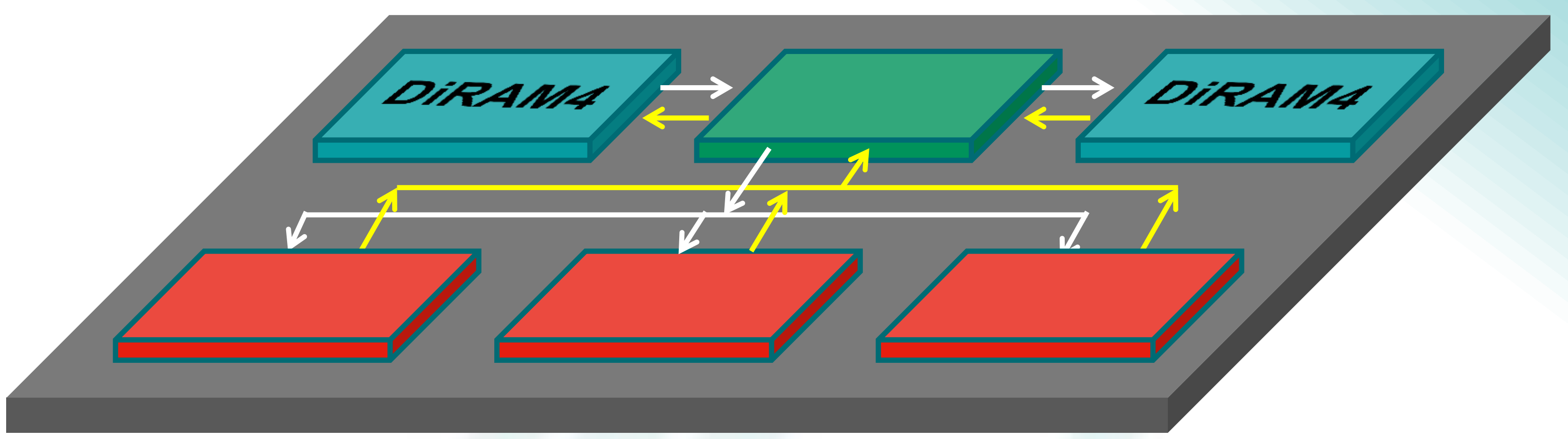
DiRAM: Efficiency for the Future

- Less aggressive wafers
- Higher array efficiency
- Much lower test cost
- Higher yield
- Longer product life cycles

Stack Density and Performance

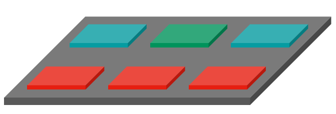
- **64 Gb** of RAM in 175 mm^2
- **256** fully independent Channels
- **16 Banks** per Channel
- **64 bit** Sep I/O Data per Channel
- **12ns tRC** (RAS to RAS in a Bank)
- **16 Tb/s Data Bandwidth**

128 Gb Supercomputer Mainstore



- Two 2.5D 1.2V CMOS I/O DiRAM4
- One Hub Chip
- Three 25Gb/s x 4 Lane SerDes

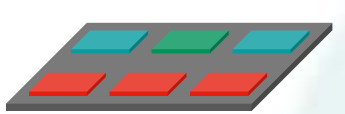
DiRAM4 vs. Hybrid Memory Cube



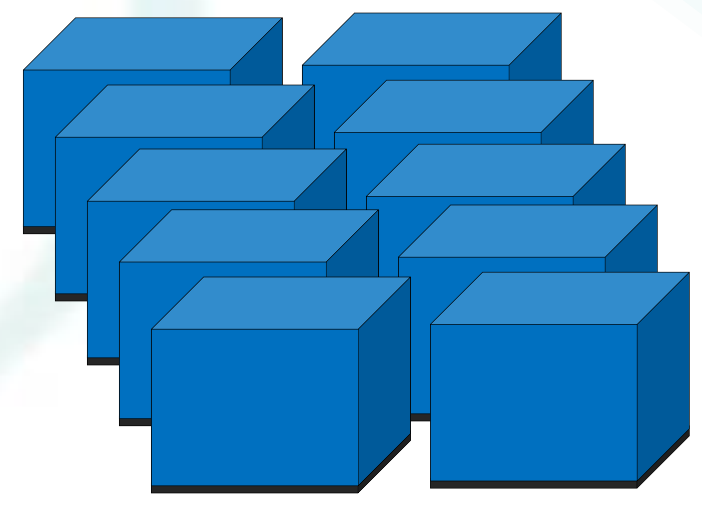
1.9x HMC for equal BANDWIDTH

1470 mm^2 Footprint (1.8x)

816 mm^2 Footprint



8x HMC for equal CAPACITY



6,272 mm^2 Footprint (7.7x)

High End Routing

Tasks

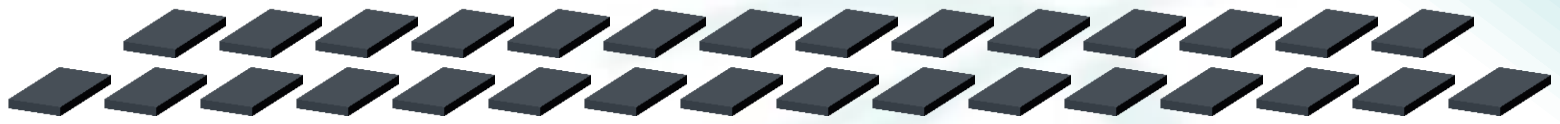
- **Packet Buffer**
  (Burst Read/Write)
- **Tables**
  (Read Dominated)
- **Stats**
  (Read-Mod-Write)

Performance Metrics

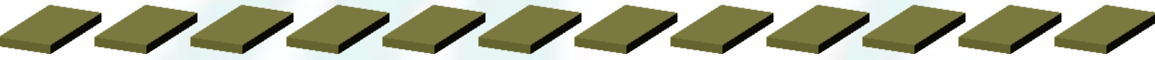
- **Density**
  - Line Rate / Seconds
- **Bandwidth**
  - Line Rate x 2.5
- **Transaction Rate**
  - Transactions x Line Rate / Min Packet Size

400Gb NP Standard RAM BOM

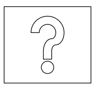
(30) 4 Gb DDR3 DRAMs = 1 Tb/s Packet Buffer



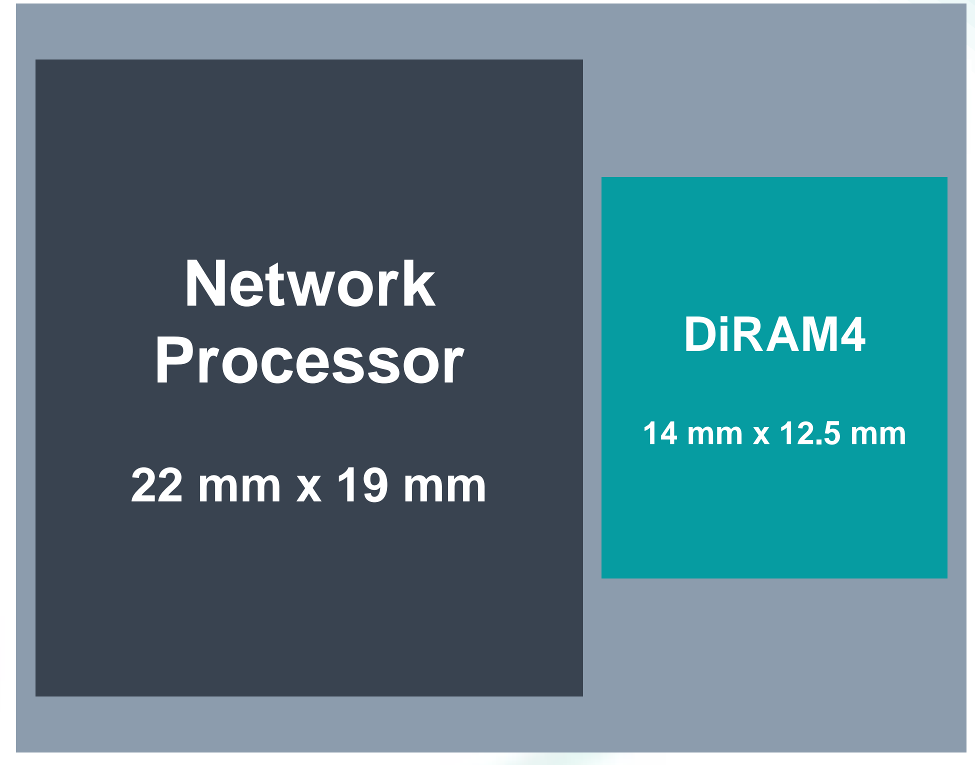
(12) 576 Mb RLDRAM3 DRAMs = 12 BT/s Tables



(4) 576 Mb SigmaQuad-IIIe SRAMs = 5 BT/s Stats



400Gb Routing with DiRAM4

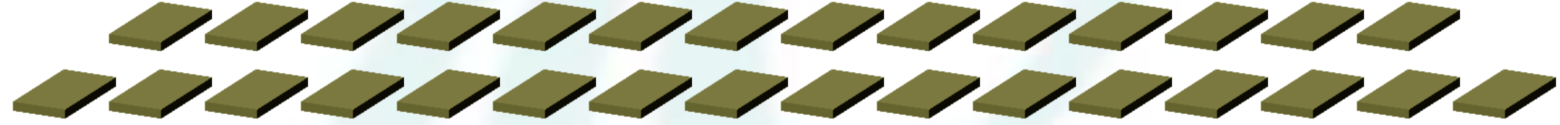


26 mm x 32 mm Interposer

1Tb NP RAM Compliment

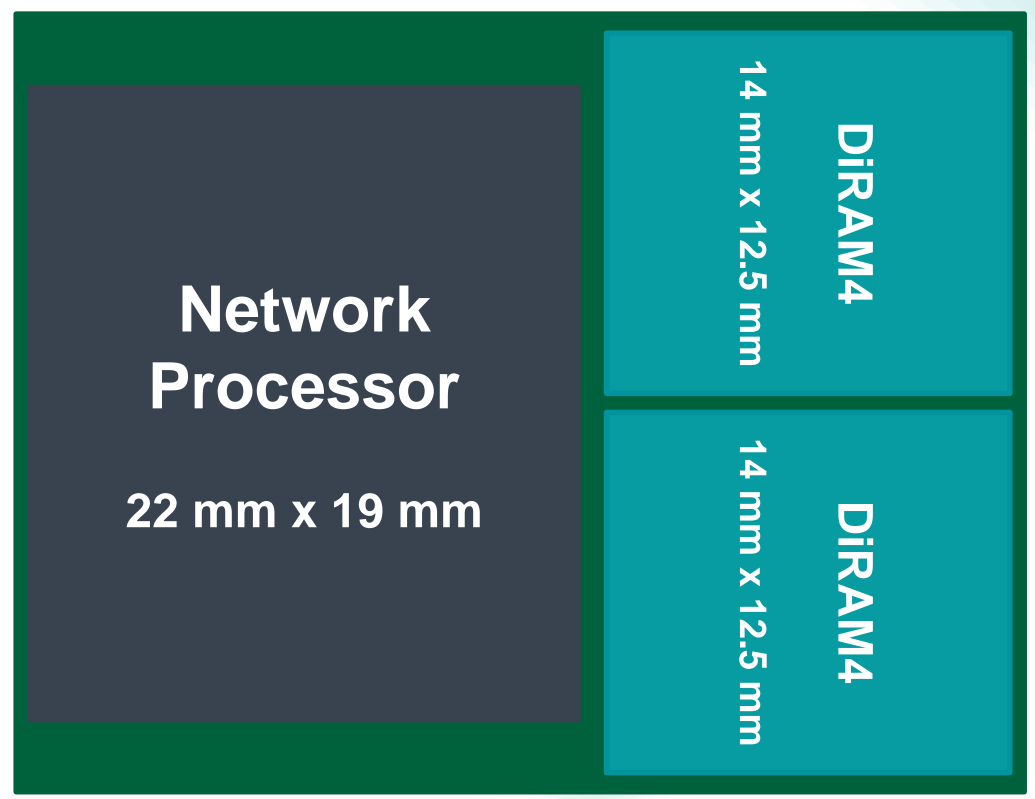
(74) 4 Gb DDR3 DRAMs = 2.5 Tb/s Packet Buffer

(30) 576 Mb RLDRAM3 DRAMs = 30 BT/s Tables



(10) 576 Mb SigmaQuad-IIIe SRAMs = 12.5 BT/s Stats

1Tb Routing with DiRAM4



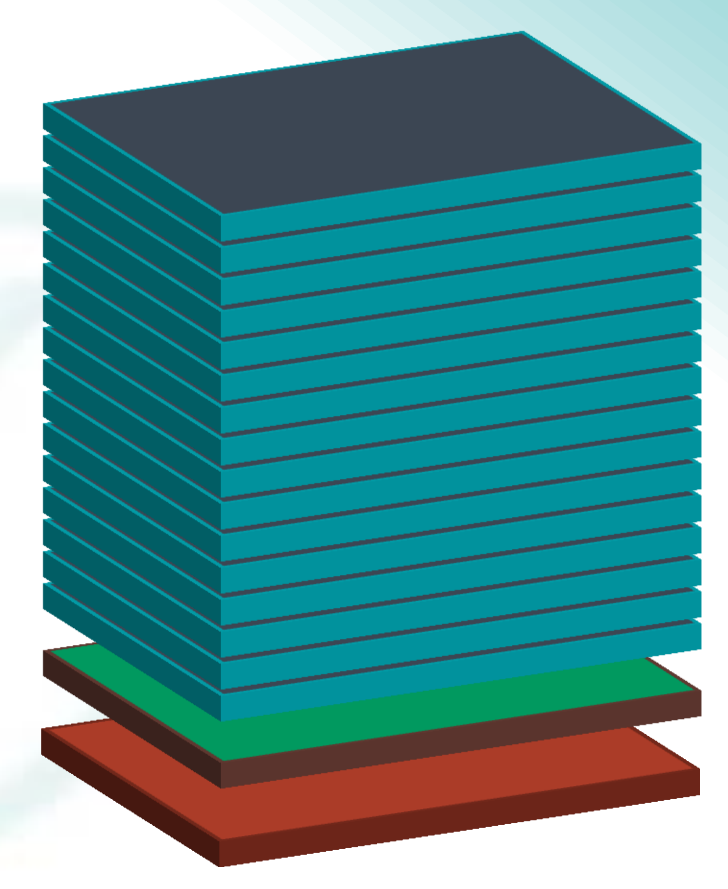
27 mm x 35 mm Interposer

The Right I/O for Each Market

DiRAM4
Launches
with
1.2 V

2.5D CMOS I/O

- Low Power
- High Performance



SerDes Over Copper

Protocol Choices	10-15 Gb/s (CRC)	25 Gb/s + (FEC / ECC)
Bulk Transfer	HMC (Micron)	DiRAM4 SCS-I
High Transaction Rate	GCI (Mosys)	DiRAM4 NS-I

Tezzaron DiRAM Roadmap

64 Tb/s

DiRAM6
256 Gb
21 ηm

32 Tb/s

DiRAM5
128 Gb
32 ηm

16 Tb/s

DiRAM4
64 Gb
45 ηm

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