

**72Mb Synchronous Quad Transfer Rate (QTRII+™) 3T-iRAM™
2.5 Cycle Read Latency**

**Burst of 4
SRAM-Compatible**

Features

- Error-resistant 3T-iRAM™ technology
- 300 MHz to 425 MHz clock
- Separate independent Read and Write data ports
- Concurrent Read/Write transactions are supported
- Dual DDRII+ interface (data rate is twice clock speed)
- Pin-compatible with QDRII+™ SRAMs
- 2.5 clock cycle Read latency
- Burst of 4 Read and Write
- Separate Port Selects for depth expansion
- Synchronous internally self-timed Writes
- Full data coherency
- 2 input clocks and 2 echo clocks
- 1.8 V ±100 mV core power supply
- 1.5 V ±100 mV I/O power supply
- HSTL I/O with variable drive output buffers
- ZQ pin for programmable output drive strength
- QVLD pin indicates valid output data
- IEEE 1149.1 JTAG-compliant Boundary Scan
- JEDEC-standard pinout and package
- 165-bump 15mm x 17mm BGA, 1 mm bump pitch
- Pin-compatible with 9Mb, 18Mb, 36Mb, and 144Mb devices

Options

- Configurations: 8M x 9 U09
4M x 18 U18
2M x 36 U36
- Package: 165 FBGA B
- Speed (MHz): 425 MHz -425
400 MHz -400
375 MHz -375
333 MHz -333
300 MHz -300
- Part number example: **TSC4Q472U18B-333**

Marking

Functional Description

3T-iRAM™ is a unique type of dynamic memory. Tezzaron has crafted these pseudo-static devices to provide entirely SRAM-compatible interfaces and timing. The unique design of these 3T memories provides soft error rates up to 10 times lower than equivalent high-speed, high-density SRAMs, while maintaining drop-in compatibility.

QTRII+™ (Quad Transfer Rate II+) is a Separate I/O architecture that makes these devices drop-in compatible with QDRII+™ SRAMs. It uses two separate ports for Read and Write operations with dedicated data input and output pins and a common address bus. This completely eliminates the “bus turn-around” time required in Common I/O devices. To maximize throughput, both data ports use DTRII+™ (Double Transfer Rate II+) interfaces.

These pipelined synchronous 72Mb devices employ two input register clocks, K and \bar{K} . These are independent single-ended clock inputs, not differential inputs, for precise data timing. Read and Write addresses are latched on alternate rising edges of the K clock. Data transfers (input and/or output) occur on the rising edges of both clocks. Two echo clocks, CQ and \bar{CQ} , simplify data capture for Reads. Writes are self-timed with on-chip circuitry.

These devices always transfer data in four packets. A0 and A1 are internally set to 0 for the first read or write transfer and automatically incremented by 1 for each of the next three transfers.

Speed Parameter Synopsis:
(all units ns)

	-425	-400	-375	-333	-300
Cycle time (tKHKH)	2.35	2.50	2.66	3.00	3.30
Access time (tKHQV)	0.45	0.45	0.45	0.45	0.45

2M x 36: Top View

11 x 15 Bump BGA – 15 x 17 mm² Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	NC/288M	SA	\overline{W}	$\overline{BW2}$	\overline{K}	$\overline{BW1}$	\overline{R}	SA	NC/144M	CQ	A
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8	B
C	D27	Q28	D19	Vss	SA	NC	SA	Vss	D16	Q7	D8	C
D	D28	D20	Q19	Vss	Vss	Vss	Vss	Vss	Q16	D15	D7	D
E	Q29	D29	Q20	VDDQ	Vss	Vss	Vss	VDDQ	Q15	D6	Q6	E
F	Q30	Q21	D21	VDDQ	VDD	Vss	VDD	VDDQ	D14	Q14	Q5	F
G	D30	D22	Q22	VDDQ	VDD	Vss	VDD	VDDQ	Q13	D13	D5	G
H	\overline{Doff}	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	D31	Q31	D23	VDDQ	VDD	Vss	VDD	VDDQ	D12	Q4	D4	J
K	Q32	D32	Q23	VDDQ	VDD	Vss	VDD	VDDQ	Q12	D3	Q3	K
L	Q33	Q24	D24	VDDQ	Vss	Vss	Vss	VDDQ	D11	Q11	Q2	L
M	D33	Q34	D25	Vss	Vss	Vss	Vss	Vss	D10	Q1	D2	M
N	D34	D26	Q25	Vss	SA	SA	SA	Vss	Q10	D9	D1	N
P	Q35	D35	Q26	SA	SA	QVLD	SA	SA	Q9	D0	Q0	P
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI	R

- Notes:** $\overline{BW0}$ controls writes to D0:D8
 $\overline{BW1}$ controls writes to D9:D17
 $\overline{BW2}$ controls writes to D18:D26
 $\overline{BW3}$ controls writes to D27:D35

4M x 18: Top View

 11 x 15 Bump BGA – 15 x 17 mm² Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	NC/144M	SA	\overline{W}	$\overline{BW1}$	\overline{K}	NC/288M	\overline{R}	SA	SA	CQ	A
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8	B
C	NC	NC	D10	Vss	SA	NC	SA	Vss	NC	Q7	D8	C
D	NC	D11	Q10	Vss	Vss	Vss	Vss	Vss	NC	NC	D7	D
E	NC	NC	Q11	VDDQ	Vss	Vss	Vss	VDDQ	NC	D6	Q6	E
F	NC	Q12	D12	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	Q5	F
G	NC	D13	Q13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	D5	G
H	\overline{Doff}	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	D14	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q4	D4	J
K	NC	NC	Q14	VDDQ	VDD	Vss	VDD	VDDQ	NC	D3	Q3	K
L	NC	Q15	D15	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q2	L
M	NC	NC	D16	Vss	Vss	Vss	Vss	Vss	NC	Q1	D2	M
N	NC	D17	Q16	Vss	SA	SA	SA	Vss	NC	NC	D1	N
P	NC	NC	Q17	SA	SA	QVLD	SA	SA	NC	D0	Q0	P
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to D0:D8
 $\overline{BW1}$ controls writes to D9:D17

8M x 9: Top View

11 x 15 Bump BGA – 15 x 17mm² Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{\text{CQ}}$	SA	SA	$\overline{\text{W}}$	NC	$\overline{\text{K}}$	NC/144M	$\overline{\text{R}}$	SA	SA	CQ	A
B	NC	NC	NC	SA	NC/288M	K	$\overline{\text{BW0}}$	SA	NC	NC	Q4	B
C	NC	NC	NC	Vss	SA	NC	SA	Vss	NC	NC	D4	C
D	NC	D5	NC	Vss	Vss	Vss	Vss	Vss	NC	NC	NC	D
E	NC	NC	Q5	VDDQ	Vss	Vss	Vss	VDDQ	NC	D3	Q3	E
F	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	F
G	NC	D6	Q6	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	G
H	$\overline{\text{Doff}}$	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q2	D2	J
K	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	K
L	NC	Q7	D7	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q1	L
M	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	NC	D1	M
N	NC	D8	NC	Vss	SA	SA	SA	Vss	NC	NC	NC	N
P	NC	NC	Q8	SA	SA	QVLD	SA	SA	NC	D0	Q0	P
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI	R

Pin Descriptions

Symbol	Type	Description	Notes
BW0 – BW3	Input	Byte write controls	Sampled on rising edges of K clocks
CQ / $\overline{\text{CQ}}$	Output	Echo clocks (active high/low)	
DN	Input	Synchronous data input	Sampled on rising edges of K clocks
$\overline{\text{Doff}}$	Input	Disable DLL (when low)	
K / $\overline{\text{K}}$	Input	Input clocks (active high/low)	
NC	---	Not connected to die or any other pin	
QN	Output	Synchronous data output	
QVLD	Output	Valid Output indicator	
$\overline{\text{R}}$	Input	Synchronous read port select (active low)	Sampled on rising edge of K
SA	Input	Synchronous address inputs	Sampled on rising edges of K clocks
TCK	Input	TAP: Test clock	For JTAG
TDI	Input	TAP: Test data input	For JTAG
TDO	Output	TAP: Test data output	For JTAG
TMS	Input	TAP: Test mode select	For JTAG
$\overline{\text{W}}$	Input	Synchronous write port select (active low)	Sampled on rising edge of K
VDD	Supply	Power supply; 1.8 V nominal	
VDDQ	Supply	Isolated output buffer supply	1.5 or 1.8 V nominal
VREF	Input	HSTL input reference voltage	
VSS	Supply	Ground	
ZQ	Input	Output impedance matching input	May be connected to VDDQ for minimum impedance
144 M	--	Available for expansion to 144 Mb	
288 M	--	Available for expansion to 288 Mb	

Functional Details

Clocks

K and $\overline{\text{K}}$ are input clocks. The rising edges of both clocks are used to capture synchronous inputs and drive out data. All accesses are initiated on the rising edge of K.

CQ and $\overline{\text{CQ}}$ are echo clocks that can be used to simplify data capture in high-speed systems. These clocks are referenced with respect to the K clocks.

Burst Operations

Read and Write operations are synchronous pipelined "burst" operations. In every case where a read or write command is accepted by the RAM, it responds by issuing or accepting four beats of data in two clock cycles, executing data transfers on subsequent rising clock edges, as illustrated in the timing diagram on page 14. It is not possible to stop a burst once it starts; four beats of data are always transferred.

Read and Write Ports

Data flows into the RAM through a dedicated Write port and out through a dedicated Read port. Address pins are multiplexed, but each port has its own dedicated registers. Read and Write operations can be conducted concurrently. Either port is deselected when its Select pin ($\overline{\text{W}}$ or $\overline{\text{R}}$) is inactive (high) at the rising edge of K; all pending operations are completed, but other inputs are ignored. Deselecting one port does not affect the other.

Read Operation

A Read is initiated by asserting \overline{R} at the rising edge of K. The address is latched at that time and stored in the Read address register. After two more rising edges of K, the first word of data is driven out onto the Q pins using \overline{K} as the timing reference; the remaining three words of data are timed by the following rises of K, \overline{K} , and K. Continuous data flow is achieved by initiating a Read on every other rising edge of K; \overline{R} is ignored on the intervening rising edges of K.

When the Read port is deselected (\overline{R} high), any active read is completed and the Q pins are tri-stated after the next rising edge of K. This allows seamless transitions without wait states between devices in a depth expanded memory.

Write Operation

A Write is initiated by asserting \overline{W} at the rising edge of K. The address is latched at that time and stored in the Write address register. At the next rising edge of K, data on the D pins is latched into a segment of the Write Data Register, subject to the values on the \overline{BWn} pins (see below). On the subsequent rising edge of \overline{K} , data on the D pins is latched into another segment of the Write Data Register, again subject to the values on the \overline{BWn} pins. The next rising edges of K and \overline{K} latch the remaining two beats of data from the D pins in the same manner. All four beats of data are then written from the Write Data Register into the specified address. Continuous data flow is achieved by initiating a Write on every other rising edge of K; \overline{W} is ignored on intervening rising edges of K.

Byte Writes

During Write operations, the \overline{BWn} (Byte Write) pins are sampled at the same time as the D pins. The values on these pins control the use of each byte of data. If a Byte Write pin is active (low), the corresponding byte of data is written; if inactive (high), the corresponding byte is ignored.

Example: x18 Write Sequence Using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0-D8	D9-D17
Beat 1	low	low	Data In	Data In
Beat 2	low	high	Data In	Ignored
Beat 3	high	high	ignored	ignored
Beat 4	high	high	ignored	ignored

Resulting Write Operation:

Byte 1 D0-D8	Byte 2 D9-D17	Byte 3 D0-D8	Byte 4 D9-D17
Written	Written	Written	Unchanged
Beat 1		Beat 2	
Unchanged	Unchanged	Unchanged	Unchanged
Beat 3		Beat 4	

Byte Write Truth Tables

\overline{BW} pins are always sampled on the same clock edge as the D pins.

H = high, L = low, X = don't care.

x36

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0-D8	D9-D17	D18-D26	D27-D35
H	H	H	H	X	X	X	X
L	H	H	H	Data	X	X	X
H	L	H	H	X	Data	X	X
L	L	H	H	Data	Data	X	X
H	H	L	H	X	X	Data	X
L	H	L	H	Data	X	Data	X
H	L	L	H	X	Data	Data	X
L	L	L	H	Data	Data	Data	X
H	H	H	L	X	X	X	Data
L	H	H	L	Data	X	X	Data
H	L	H	L	X	Data	X	Data
L	L	H	L	Data	Data	X	Data
H	H	L	L	X	X	Data	Data
L	H	L	L	Data	X	Data	Data
H	L	L	L	X	Data	Data	Data
L	L	L	L	Data	Data	Data	Data

x18

$\overline{BW0}$	$\overline{BW1}$	D0 - D8	D9 - D17
H	H	X	X
L	H	Data	X
H	L	X	Data
L	L	Data	Data

Concurrent Transactions

The Read and Write ports are completely independent, so the user can access any location on either port regardless of the status of the other port. When both ports access the same address in successive clock cycles, a Read can forward the data from a Write that was initiated on the previous rising edge of K.

Reads and Writes cannot be started in the same clock cycle. A continuous data flow is maintained in both directions by initiating Read and Write transactions on alternate rising edges of K. If both ports are disabled (\overline{R} and \overline{W} high) and the user asserts both \overline{R} and \overline{W} at the same time, the Read receives priority. If both \overline{R} and \overline{W} are held low, continuous concurrent Reads and Writes occur until either signal is taken high.

Initiating Transactions

Clock Edge	Read Port Status	Write Port Status	\overline{R}	\overline{W}	Result
$\uparrow K$	Idle (disabled) –or– Read initiated on 2 nd previous $\uparrow K$	Any	Low	Any	Read operation begins, using address on SA pins.
$\uparrow K$	Read initiated on previous $\uparrow K$	Any	Low	Low	Write operation begins, using address on SA pins.
$\uparrow K$	Any	Idle (disabled) –or– Write initiated on 2 nd previous $\uparrow K$	High	Low	Write operation begins, using address on SA pins.
$\uparrow K$	Any	Write initiated on previous $\uparrow K$	High	Low	No new operation begins.
$\uparrow K$	Any	Any	High	High	No new operation begins.

Note: In all cases, operations already in progress are completed

Truth Table

Operation	Clock Edge	\bar{R}	\bar{W}	SA	Data	Notes
Write	$\uparrow K$	H	L	Write Address	X	1, 2
	$\uparrow \bar{K}$	X	X	X	X	
	$\uparrow K$	X	X	X	D (Write Address)	3
	$\uparrow \bar{K}$	X	X	X	D (Write Address + 1)	
	$\uparrow K$	X	X	X	D (Write Address + 2)	4
	$\uparrow \bar{K}$	X	X	X	D (Write Address + 3)	
Read	$\uparrow K$	L	X	Read Address	X	5
	$\uparrow \bar{K}$, then $\uparrow K$	X	X	X	X	6
	$\uparrow \bar{K}$, $\uparrow K$, $\uparrow \bar{K}$	X	X	X	X	7
	$\uparrow K$	X	X	X	Q (Read Address)	6
	$\uparrow \bar{K}$	X	X	X	Q (Read Address + 1)	
	$\uparrow K$	X	X	X	Q (Read Address + 2)	7
	$\uparrow \bar{K}$	X	X	X	Q (Read Address + 3)	
NOP (Deselect)	$\uparrow K$	H	H	X	Pending transactions finish, then D = X, Q = High-Z	
Standby	Stopped	X	X	X	D and Q = Previous State	

Notes: X = don't care; H = logic high; L = logic low; \uparrow represents rising edge.

- 1: Assumes that no Write was initiated on the previous $\uparrow K$.
- 2: \bar{R} may be low if a Read was initiated on the previous $\uparrow K$.
3. A Read may be initiated here.
4. Another Write may be initiated here.
5. Assumes that no Read was initiated on the previous $\uparrow K$.
6. A Write may be initiated on the $\uparrow K$.
7. Another Read may be initiated on the $\uparrow K$.

Programmable Impedance

An optional programmable impedance output driver can periodically adjust the impedance to compensate for drifts in supply voltage and temperature. To disable this feature, tie the ZQ pin directly to VDDQ. The device then runs with a constant minimum impedance.

To enable the feature, connect the ZQ pin to Vss via an external resistor, RQ, with a value 5x the desired output impedance. The allowable range of RQ is between 175 Ω and 350 Ω with VDDQ = 1.5V. An internal calibration sequence occurs every 1024 cycles and an update is performed during the next available deselected memory cycle. Each update may move the impedance level one step toward the optimum level.

QVLD

The QVLD signal is provided to simplify data capture. It is edge-aligned with the echo clock and follows the timing of any data pin. This signal is asserted high one-half cycle before output (Read) data arrives at the Q pins, and it goes low one-half cycle before the output pins are tri-stated.

DLL (Delay Lock Loop)

This device's DLL is designed to function between 80 MHz and the specified maximum clock frequency. The DLL may be disabled by applying ground to the $\overline{\text{Doff}}$ pin; however, operation without the DLL will cause longer access times.

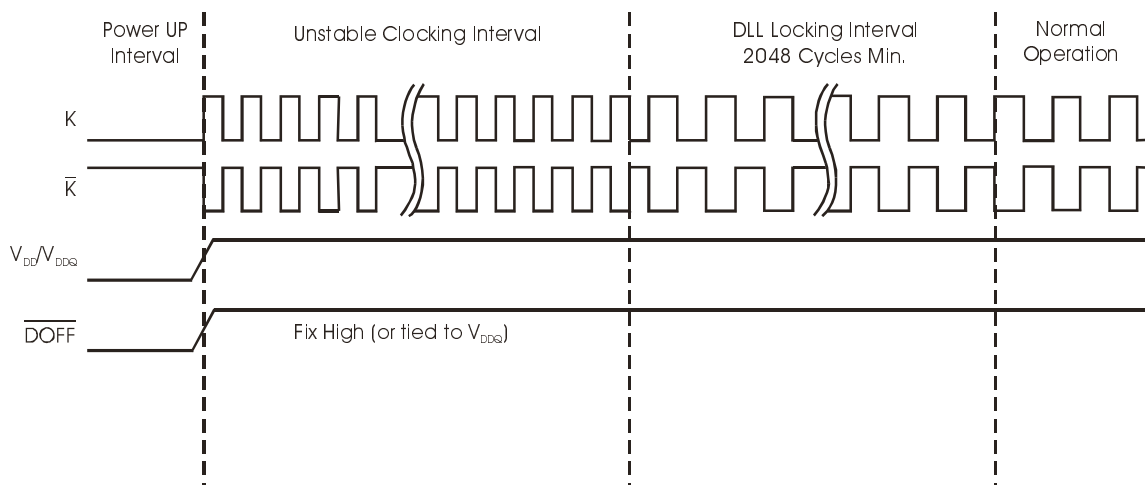
To use the DLL, pull $\overline{\text{Doff}}$ high with a pullup resistor of 1 Kohm. At power-up or reset the DLL locks to the K clock within 2048 cycles of stable clock. During operation, it synchronizes to the K clock, so this clock must have low phase jitter (see t_{KCVar} on page 13). After power-up, the DLL can be reset either by taking $\overline{\text{Doff}}$ low for 30 ns and then bringing it high, or else by preventing a rising K clock edge for at least 30 ns and then providing stable clock for 2048 cycles. If the DLL loses its lock during operation, a reset is not necessary; it re-locks automatically within 2048 clock cycles after a stable clock is presented.

Power-Up Sequence

To prevent undefined operations, power up the device in this sequence:

1. Apply power with $\overline{\text{Doff}}$ high (all other inputs are "don't care").
2. Apply VDD before VDDQ.
3. Apply VDDQ before VREF, or at the same time as VREF.
4. Allow power and clocks to stabilize, then wait 2048 clocks to ensure DLL lock.

Power-Up Waveforms



Absolute Maximum Ratings

Description	Value	Unit
Supply voltage on VDD pins relative to VSS	-0.5 to 2.9	V
Supply voltage on VDDQ pins relative to VSS	-0.5 to VDD	V
DC output voltage in High-Z state	-0.5 to VDDQ +0.5	V
DC input voltage (subject to overshoot/undershoot, see below)	-0.5 to VDD +0.5	V
Static discharge voltage (per MIL-STD-883, method 3015)	> 2001	V
Input current	+/- 40	mA dc
Output current (low)	+/- 40	mA dc
Latch-up current	>200	mA dc
Storage temperature	-65 to 150	°C
Ambient temperature (power applied)	-55 to +125	°C
Operating temperature (VDD 1.8V ±0.1V and VDDQ 1.5V ±0.1V, assuming linear ramp at power-up within 200 ms, with VIH < VDD and VDDQ • VDD.)	0 to 70	°C
Overshoot: VIH(AC) < VDDQ + 0.85V, pulse width < tKHKH/2 Undershoot: VIL(AC) > -1.5V, pulse width < tKHKH/2		

Note: Permanent damage to the device may occur if the Maximum Ratings are exceeded.

Electrical Characteristics

Over the operating range (0°C to 70°C), all voltages referenced to Ground

DC Voltage

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Supply voltage		1.7	1.8	1.9	V
VDDQ	I/O Supply voltage		1.4	1.5	1.6	V
VOH	Output high voltage	Impedance controlled, IOH = -(VDDQ/2)/(RQ/5), 175• ≤ RQ ≤ 350•	VDDQ/2 - 0.12		VDDQ/2 + 0.12	V
		Nominal impedance, IOH = -0.1 mA	VDDQ - 0.2		VDDQ	V
VOL	Output low voltage	Impedance controlled, IOL = (VDDQ/2)/(RQ/5), 175• ≤ RQ ≤ 350•	VDDQ/2 - 0.12		VDDQ/2 + 0.12	V
		Nominal impedance, IOL = 0.1 mA	VSS		0.2	V
VIH	Input high voltage	Overshoot: VIH(AC) < VDDQ + 0.85V, pulse width < tKHKH /2 Undershoot: VIL(AC) > -1.5V, pulse width < tKHKH /2	VREF + 0.1		VDDQ + 0.3	V
VIL	Input low voltage		- 0.3		VREF - 0.1	V
VREF	Reference voltage		Greater of: 0.68 or 0.46 * VDDQ	0.75	Lesser of: 0.85 or 0.54 * VDDQ	V

DC Current

Parameter	Description	Test Conditions	Speed	Min	Max	Unit
I _x	Input leakage current	Ground <= V _I <= V _{DDQ}		-5	5	•A
I _{oz}	Output leakage current	Ground <= V _I <= V _{DDQ} , output disabled		-5	5	•A
I _{DD}	V _{DD} operating supply	V _{DD} = max, I _{OUT} = 0 mA, f = f _{MAX} = 1/ t _{KHKH}	425 MHz	tbd	tbd	mA
			400 MHz	tbd	tbd	mA
			375 MHz	tbd	tbd	mA
			333 MHz	tbd	tbd	mA
			300 MHz	tbd	tbd	mA
I _{SB1}	Automatic power-down current	Both ports deselected, Inputs static, V _{DD} = max, V _{IN} >= V _{IH} or V _{IN} <= V _{IL} , f = f _{MAX} = 1/ t _{KHKH}	425 MHz	tbd	tbd	mA
			400 MHz	tbd	tbd	mA
			375 MHz	tbd	tbd	mA
			333 MHz	tbd	tbd	mA
			300 MHz	tbd	tbd	mA

AC Input Requirements

Parameter	Description	Min	Max	Unit
V _{IH}	Input high voltage	V _{REF} + 0.2	--	V
V _{IL}	Input low voltage	--	V _{REF} - 0.2	V

To guarantee AC characteristics, V_{IL}, V_{IH}, Trise, and Tfall of inputs and clocks must be within 10% of each other.

Capacitance

These parameters tested initially and after any design or process change that may affect them

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C f = 1 MHz V _{DD} = 1.8 V V _{DDQ} = 1.5 V	5	pF
C _{CLK}	Clock input capacitance		7	pF
C _O	Output capacitance		6	pF

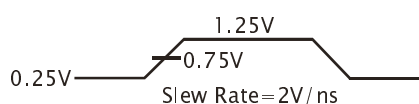
Thermal Resistance

These parameters tested initially and after any design or process change that may affect them

Parameter	Symbol	Test conditions	165 FBGA Package	Unit
Junction to Ambient	•JA	Standard test methods and procedures for thermal impedance per EIA / JESD51	tbd	°C/W
Junction to Case	•JC		tbd	°C/W

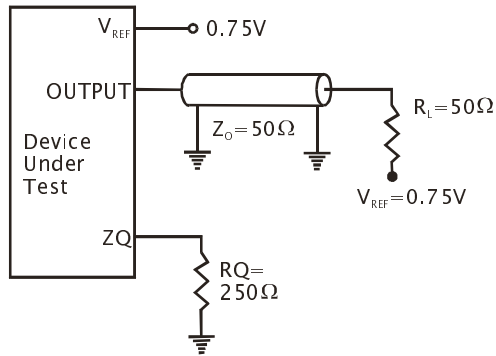
AC Waveform

(All input pulses)



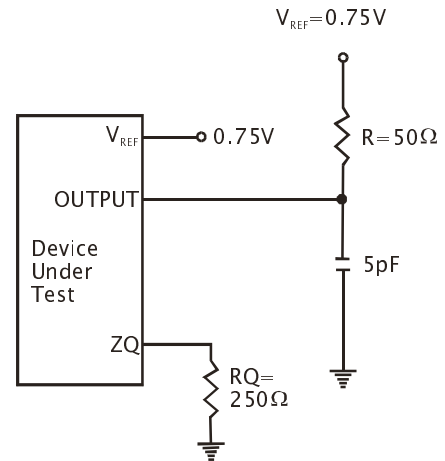
AC Test Loads

VDDQ = 1.5V



TEST CONFIGURATION "A"

Applies to all measurements unless specified otherwise.



TEST CONFIGURATION "B"

Output load as shown includes jig and scope.
Applies only to the measurement of tKHQZ and tKHQX1.

Switching Characteristics

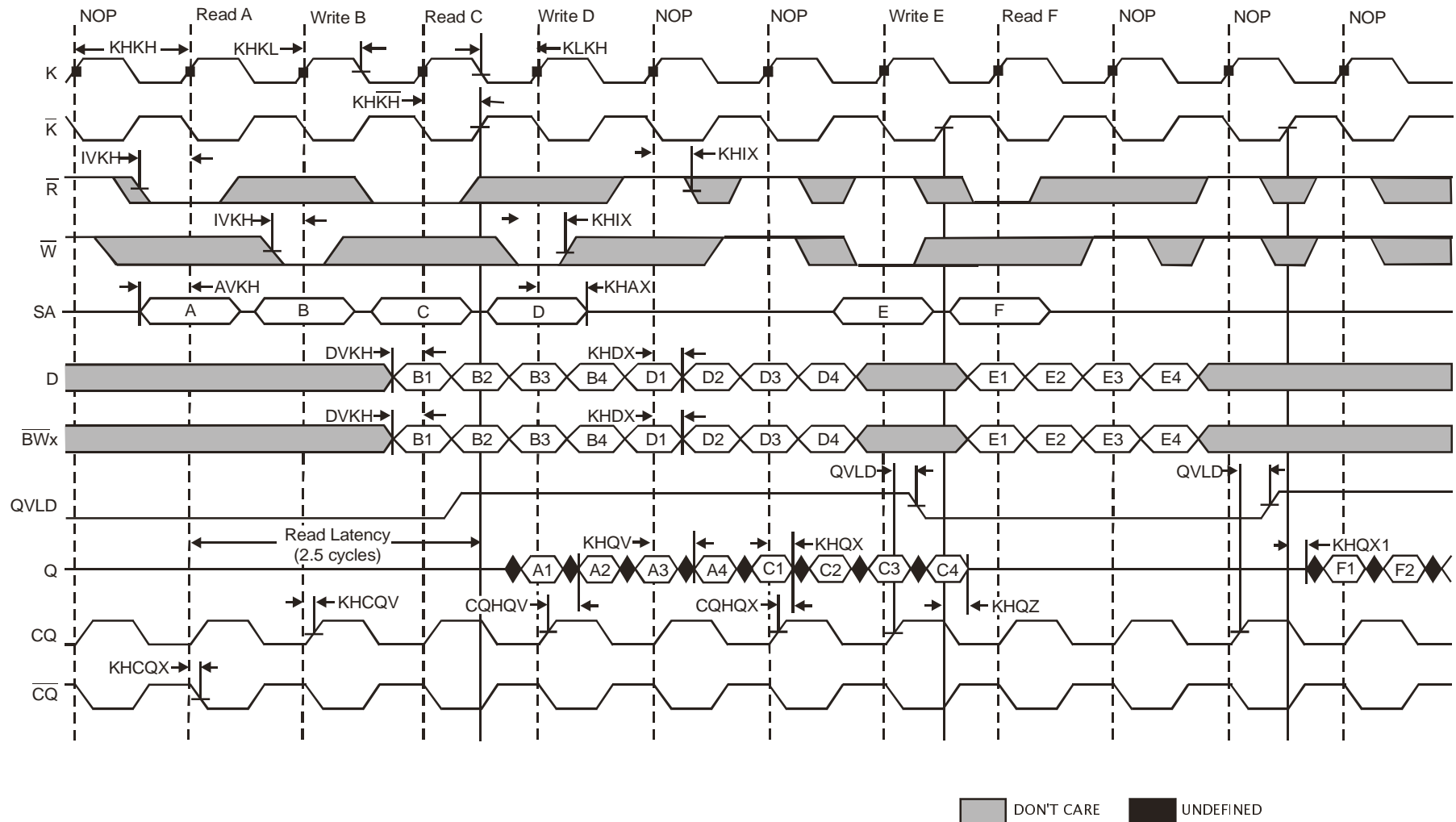
All measurements in ns unless specified otherwise

Parameter	Symbol	425 MHz		400 MHz		375 MHz		333 MHz		300 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
VDD valid to first read/write access	tPOWER	minimum: 1 ms									
Clock Timing											
K / \bar{K} clock cycle time	tKHKH	2.35	3.05	2.50	3.25	2.66	3.46	3.00	3.90	3.30	4.20
K / \bar{K} clock high pulse width	tKHKL	0.40	--	0.40	--	0.40	--	0.40	--	0.40	--
K / \bar{K} clock low pulse width	tKCLKH	0.40	--	0.40	--	0.40	--	0.40	--	0.40	--
K rise to \bar{K} rise	tKHKH	1.00	--	1.06	--	1.13	--	1.28	--	1.40	--
Output Timing											
K / \bar{K} rise to output data valid	tKHQV	--	0.45	--	0.45	--	0.45	--	0.45	--	0.45
K / \bar{K} rise to output data hold	tKHQX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.45	--
K / \bar{K} rise to echo clock valid	tKHCQV	--	0.45	--	0.45	--	0.45	--	0.45	--	0.45
K / \bar{K} rise to echo clock hold	tKHCQX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.45	--
CQ, \bar{CQ} rise to data valid	tCOHQV	--	0.20	--	0.20	--	0.20	--	0.20	--	0.20
CQ, \bar{CQ} rise to data hold	tCOHQX	-0.20	--	-0.20	--	-0.20	--	-0.20	--	-0.20	--
K / \bar{K} rise to High-Z [note 3]	tKHQZ	--	0.45	--	0.45	--	0.45	--	0.45	--	0.45
K / \bar{K} rise to Low-Z [note 3]	tKHQX1	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.45	--
CQ, \bar{CQ} rise to QVLD rise or fall	tQVLD	-0.20	0.20	-0.20	0.20	-0.20	0.20	-0.20	0.20	-0.20	0.20
Setup Timing											
Address setup to K rise	tAVKH	0.40	--	0.40	--	0.40	--	0.40	--	0.40	--
\bar{R} / \bar{W} setup to K / \bar{K} rise	tIVKH	0.40	--	0.40	--	0.40	--	0.40	--	0.40	--
Input data and $\bar{B}Wn$ setup to K / \bar{K} rise	tDVKH	0.28	--	0.28	--	0.28	--	0.28	--	0.28	--
Hold Timing											
Address hold after K rise	tKHAX	0.40	--	0.40	--	0.40	--	0.40	--	0.40	--
\bar{R} / \bar{W} hold after K / \bar{K} rise	tKHIX	0.40	--	0.40	--	0.40	--	0.40	--	0.40	--
Input data and $\bar{B}Wn$ hold after K / \bar{K} rise	tKHDX	0.28	--	0.28	--	0.28	--	0.28	--	0.28	--
DLL Timing											
Clock phase jitter	tKCVar	--	0.20	--	0.20	--	0.20	--	0.20	--	0.20
DLL lock time	tKCLock	minimum: 2048 clock cycles									
K static (>VIH or <VIL) to DLL reset	tKCRReset	30	--	30	--	30	--	30	--	30	--

Notes:

1. All measurements are over the operating range (0°C to 70°C)
2. Any part may be operated at a frequency lower than its defined speed rating. In this case, the part requires the input timings of that frequency, and outputs data with the output timings of that frequency.
3. tKHQZ and tKHQX1 use test configuration "B" (see page 12). Transition is measured ±100 mV from steady-state voltage. tKHQZ is always less than tKHQX1, and tKHQX1 is always less than tKHQV.

Timing Diagram



Note: If address B is the same as address C, then data B1/B2/B3/B4 will be the same as data C1/C2/C3/C4.
If address A is the same as address B, data A1/A2/A3/A4 will be read from the device before data B1/B2/B3/B4 are written (posted write).

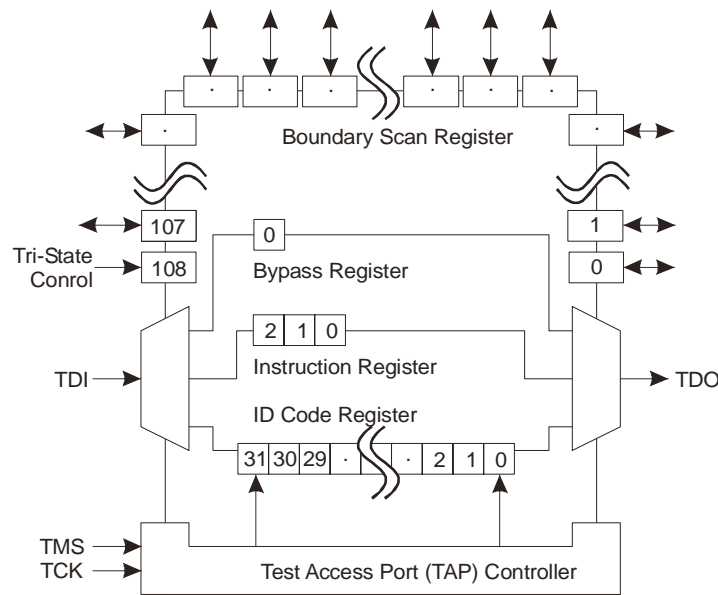
JTAG Port Operation

Overview

This device incorporates a serial boundary scan interface that complies with IEEE Standard 1149.1-1990, commonly known as JTAG. The JTAG Port is also known as a Test Access Port, or TAP. It can be used to read the device ID code, monitor all RAM input and I/O pads, drive pre-loaded values into the I/O bus, or the I/O bus to a High-Z state.

The port's input interface levels scale with VDD and the output drivers are powered by VDDQ. The port is reset at power-up and remains inactive until clocked. Pins, registers, states, and instructions are described below.

JTAG Test Access Port Block Diagram



JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all events. Inputs are captured on the rising edge; outputs are driven on the falling edge.
TMS	Test Mode Select	In	Command input for the JTAG state machine, sampled on the rising edge of TCK.
TDI	Test Data In	In	The input side of any selected register, sampled on the rising edge of TCK.
TDO	Test Data Out	Out	The output side of any selected register, driven on the falling edge of TCK.

Notes: TCK, TDI, and TMS have internal pull-up circuits; when undriven they produce a logic one input level.

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The JTAG controller is reset automatically at power-up, and again whenever it enters the Test-Logic-Reset state.

The "selected" register is determined by the current instruction and the state of the JTAG controller.

Disabling the JTAG Port

For normal operation of the device without using JTAG, the controller can be held in a permanent Reset state. To do this, TCK, TDI, and TMS are left floating or tied to either VDD or VSS. TDO should be left unconnected.

JTAG Registers

The JTAG interface has four serial shift registers that are used in conjunction with JTAG instructions. When a register is selected, it is placed between TDI and TDO so that it can shift data out serially on the falling edges of TCK and capture input data on the rising edges of TCK, depending on the state of the controller.

Instruction Register

The three-bit Instruction Register holds an instruction to be executed. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller enters the Test-Logic-Reset state. The user may load instructions through the TDI pin using the various IR (Instruction Register) states. The Instruction Register is always selected in the IR states, regardless of the current instruction.

Bypass Register

The single-bit Bypass Register can be placed between TDI and TDO to pass serial data through the JTAG Port with as little delay as possible. The Bypass Register is selected by the BYPASS instruction.

Identification (ID) Register

The 32-bit ID Register receives an identification code from an on-chip ID ROM. The code describes various attributes of the RAM as indicated in the table below. The ID Register is selected by the IDCODE instruction.

ID Code Contents

Bit#	Die Revision Code				Not Used								I/O Configuration								Tezzaron Semiconductor JEDEC Vendor ID Code								Presence Register			
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4		3	2	1
x9	X	X	X	X	0	0	0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	0	0	0	1	0	1	1	0	0	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	0	0	0	1	0	1	1	0	0	1
x36	X	X	X	X	0	0	0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	0	0	0	1	0	1	1	0	0	1

Boundary Scan Register

The Boundary Scan Register is a chain of 109 cells. Each cell contains a Scan bit and an Update bit. The Scan bits can capture the logic level found on the RAM's I/O pins; the Update bits can drive a preloaded set of data onto the RAM's outputs. The Boundary Scan Register cells are daisy chained together so their contents can be shifted out serially through the TDO pin and loaded through the TDI pin. The relationship between the device pins and the cells in the Boundary Scan Register is described in the Scan Order Table below; note that the register includes a number of special purpose cells that do not represent I/O pins. The Boundary Scan Register is selected by the SAMPLE-Z, SAMPLE/PRELOAD, and EXTEST instructions.

Scan Order Table

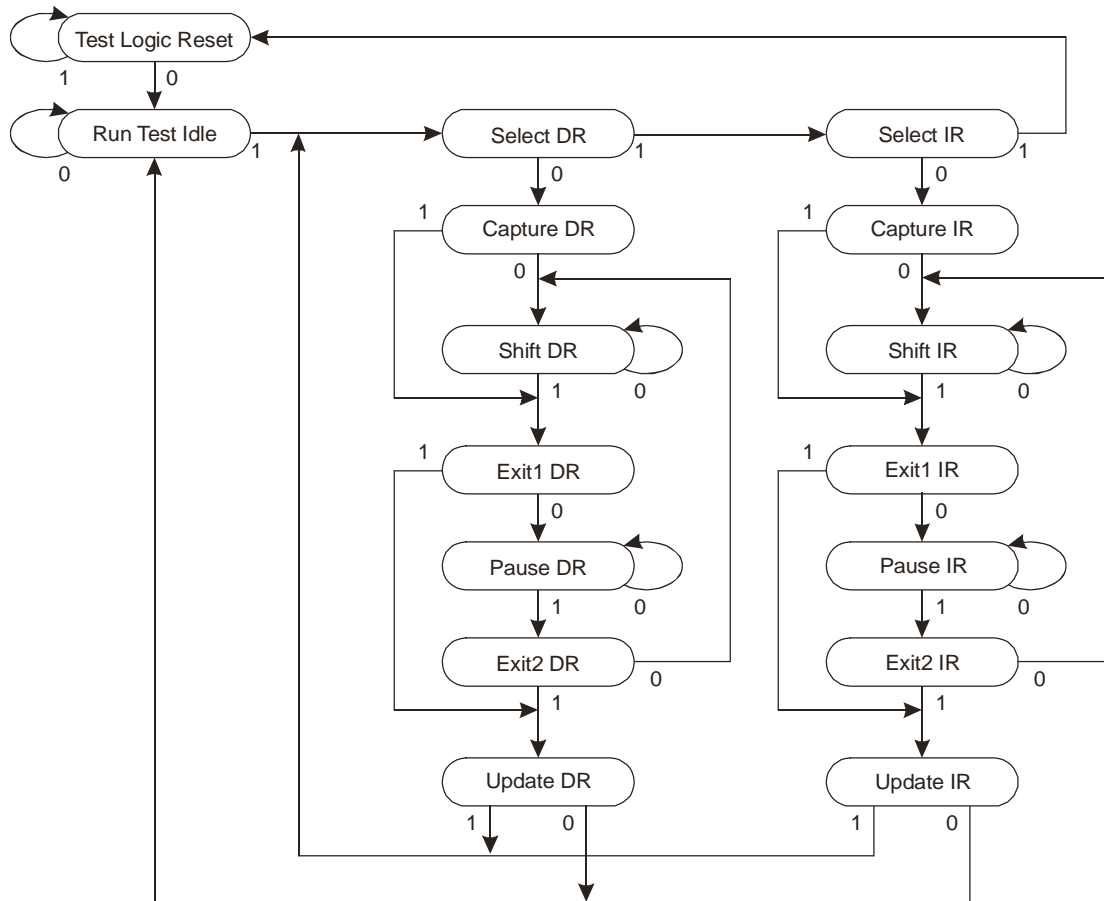
Cell#	Pin Name	I/O	Notes
0	tbd	tbd	
1	tbd	tbd	
2	tbd	tbd	
3	tbd	tbd	
4	tbd	tbd	
5	tbd	tbd	
6	tbd	tbd	
7	tbd	tbd	
8	tbd	tbd	
9	tbd	tbd	
10	tbd	tbd	
11	tbd	tbd	
12	tbd	tbd	
13	tbd	tbd	
14	tbd	tbd	
15	tbd	tbd	
16	tbd	tbd	
17	tbd	tbd	
18	tbd	tbd	
19	tbd	tbd	
20	tbd	tbd	
21	tbd	tbd	
22	tbd	tbd	
23	tbd	tbd	
24	tbd	tbd	
25	tbd	tbd	
26	tbd	tbd	
27	tbd	tbd	

Cell#	Pin Name	I/O	Notes
28	tbd	tbd	
29	tbd	tbd	
30	tbd	tbd	
31	tbd	tbd	
32	tbd	tbd	
33	tbd	tbd	
34	tbd	tbd	
35	tbd	tbd	
36	tbd	tbd	
37	tbd	tbd	
38	tbd	tbd	
39	tbd	tbd	
40	tbd	tbd	
41	tbd	tbd	
42	tbd	tbd	
43	tbd	tbd	
44	tbd	tbd	
45	tbd	tbd	
46	tbd	tbd	
47	tbd	tbd	
48	tbd	tbd	
49	tbd	tbd	
50	tbd	tbd	
51	tbd	tbd	
52	tbd	tbd	
53	tbd	tbd	
54	tbd	tbd	
55	tbd	tbd	

Cell#	Pin Name	I/O	Notes
56	tbd	tbd	
57	tbd	tbd	
58	tbd	tbd	
59	tbd	tbd	
60	tbd	tbd	
61	tbd	tbd	
62	tbd	tbd	
63	tbd	tbd	
64	tbd	tbd	
65	tbd	tbd	
66	tbd	tbd	
67	tbd	tbd	
68	tbd	tbd	
69	tbd	tbd	
70	tbd	tbd	
71	tbd	tbd	
72	tbd	tbd	
73	tbd	tbd	
74	tbd	tbd	
75	tbd	tbd	
76	tbd	tbd	
77	tbd	tbd	
78	tbd	tbd	
79	tbd	tbd	
80	tbd	tbd	
81	tbd	tbd	
82	tbd	tbd	
83	tbd	tbd	

Cell#	Pin Name	I/O	Notes
84	tbd	tbd	
85	tbd	tbd	
86	tbd	tbd	
87	tbd	tbd	
88	tbd	tbd	
89	tbd	tbd	
90	tbd	tbd	
91	tbd	tbd	
92	tbd	tbd	
93	tbd	tbd	
94	tbd	tbd	
95	tbd	tbd	
96	tbd	tbd	
97	tbd	tbd	
98	tbd	tbd	
99	tbd	tbd	
100	tbd	tbd	
101	tbd	tbd	
102	tbd	tbd	
103	tbd	tbd	
104	tbd	tbd	
105	tbd	tbd	
106	tbd	tbd	
107	tbd	tbd	
108	Tri-State Control	n/a	

JTAG Controller State Diagram



JTAG Controller States

Overview

The JTAG controller is inactive until clocked with TCK. When TCK is activated, the controller is in the Test Logic Reset state. Subsequent transitions between states are controlled by the TMS signal as shown in the diagram above. TMS is sampled at each rising edge of TCK.

The DR states select and manipulate the four JTAG data registers; the IR states select and manipulate the Instruction Register.

Test Logic Reset

In this state, the IDCODE instruction is loaded into the Instruction Register, no control is exerted over the RAM's output pins, and the RAM executes as if the JTAG port were disabled. If TMS is held at 1 for five cycles, the controller returns to this state and loops until it detects a TMS value of 0.

Run Test Idle

This is the entry point for all instructions. The controller can loop here as needed, but performs no functions.

Select DR

The controller selects a data register (determined by the current instruction) and places it between TDI and TDO.

Capture DR

Depending upon the current instruction, the selected register may receive data from sources other than TDI.

Shift DR

On the falling edge of TCK, the least significant bit of the selected register is shifted onto TDO. On the rising edge of TCK, the value on the TDI pin is captured and shifted into the most significant bit of the selected register.

Exit1 DR

Data movement stops. No function is performed.

Pause DR

The controller can loop here, but performs no functions.

Exit2 DR

No function is performed.

Update DR

If the current instruction is SAMPLE or EXTEST, data in the Boundary Scan Register is copied from the Scan bits to the Update bits. Otherwise, no function is performed.

Select IR

The Instruction Register is selected and placed between TDI and TDO.

Capture IR

The controller loads the two least significant bits of the Instruction Register with 01.

Shift IR, Exit1 IR, Pause IR, Exit2 IR

These states are analogous to Shift DR, Exit1 DR, Pause DR, and Exit2 DR.

Update IR

Instruction loading is complete; the instruction is decoded for implementation. If the new instruction is EXTEST or SAMPLE-Z, JTAG exerts control over the RAM's output pins; otherwise, it releases control of those pins.

JTAG Controller Instruction Set

Instruction Summary

Instruction	Binary Code	Description
EXTEST	000	Either drives contents onto RAM outputs or forces outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
IDCODE	001	Selects and loads ID Register; allows reading of register. Default instruction – automatically loaded in test-logic-reset state.
SAMPLE-Z	010	Forces all RAM outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading of Boundary Scan Register.
RFU	011	Do not use this instruction; reserved for future use. (Currently replicates BYPASS instruction.)
SAMPLE/PRELOAD	100	Selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
TEZZARON	101	Tezzaron private instruction; do not use.
RFU	110	Do not use this instruction; Reserved for Future Use. (Currently replicates BYPASS instruction.)
BYPASS	111	Selects Bypass Register; allows rapid pass-through of data.

Instruction Descriptions

NOTE: Several of these instructions capture signals from the RAM's I/O ring. The user must be aware that the JTAG clock (TCK) operates at 20 MHz or less, while the RAM clock operates more than an order of magnitude faster. Because of the difference in clock frequencies, it is possible that an input or output will undergo a transition during the capture. In this case, the signal may be captured while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured, and repeatable results may not be possible. To guarantee that the correct value of a signal is captured, the signal must be stabilized long enough to meet the JTAG set-up plus hold times ($t_{TS} + t_{TH}$). If there is no way in a design to stop (or slow) the RAM clock, the RAM clock inputs might not be captured correctly; however, it is still possible to capture all other signals and simply ignore the captured values of the RAM clock signals.

BYPASS

This instruction allows test data to pass through the device with minimal delay, to facilitate testing of other devices on the scan path.

Select-DR: The Bypass Register is placed between TDI and TDO.

Shift-DR: Data is shifted out through TDO and in from TDI.

SAMPLE/PRELOAD

This instruction allows sample data to be captured and examined without interfering with normal device operation. It also allows test data to be pre-loaded for later use with the EXTEST instruction.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data from the Scan bits is copied into the Update bits for later use (see EXTEST).

EXTEST

This instruction captures sample data and sets up test data, much like SAMPLE/PRELOAD, but it also controls the RAM's output pins. EXTEST is for testing only, as it disrupts normal operation of the device. As soon as the EXTEST instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded. The values in the Boundary Scan Register's Update bits are driven onto the output pins, *unless the Tri-State Control cell has been set (see below)*, in which case the output pins are tri-stated.

EXTEST and Tri-State

The Boundary Scan Register's last cell, #108, is the Tri-State Control cell. During EXTEST, it directly controls the state of the RAM's output pins. When HIGH, it enables the Update bit values to drive the output bus; when LOW, it places the output bus into a High-Z condition. The Tri-State Control cell's value is set to HIGH whenever the controller is in the "Test-Logic-Reset" state. The value is changed with the SAMPLE/PRELOAD or EXTEST instruction by shifting the desired value into the cell during the Shift-DR state. During Update-DR, the new value is copied into the cell's Update bit. From there, it controls the EXTEST instruction's behavior.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data in the Scan bits is copied to the Update bits. The values take effect immediately, driving the RAM's output bus as directed.

IDCODE

IDCODE is the default instruction, loaded automatically whenever the controller is placed in the Test-Logic-Reset state. It allows access to the device's internal ID ROM contents.

Select-DR: The ID Register is placed between TDI and TDO.

Capture-DR: The ID Register is loaded with the device's 32-bit identification code from the ID ROM.

Shift-DR: The contents of the ID Register is shifted out through TDO.

SAMPLE-Z

This instruction functions somewhat like EXTEST, except that the output bus is always tri-stated and the Update bits are not changed. Like EXTEST, it is disruptive to normal device operation. As soon as the SAMPLE-Z instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded.

Select-DR: The Boundary Scan Register is connected between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits.

Shift-DR: Data in the Scan bits is shifted out serially through TDO.

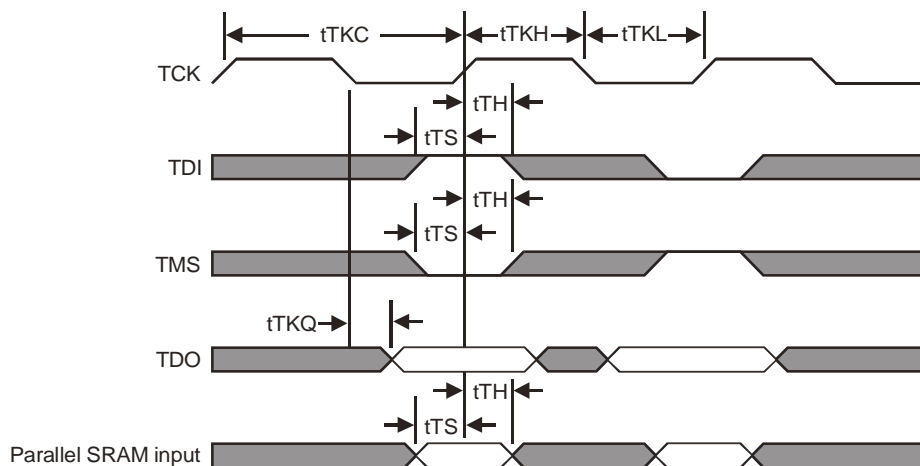
Tezzaron

This instruction is reserved for vendor use; do not use.

RFU

This instruction is reserved for future use; in this device it replicates the BYPASS instruction.

JTAG Port Timing Diagram



JTAG Port Recommended Operating Conditions and DC Characteristics (V)

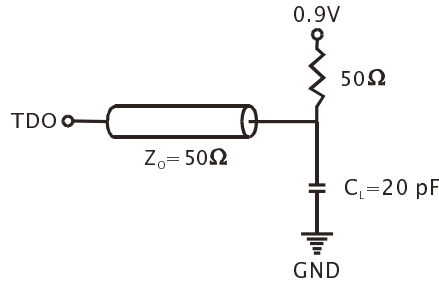
Parameter	Symbol	Min.	Typ.	Max.
Power Supply Voltage	VDDQ	1.7	1.8	1.9
Input High Voltage	V _{IH}	1.3	--	VDD + 0.3
Input Low Voltage	V _{IL}	-0.3	--	0.5
Output High Voltage (I _{OH} = -2 mA)	V _{OH}	1.4	--	VDD
Output Low Voltage (I _{OL} = 2 mA)	V _{OL}	V _{SS}	--	0.4

Note: During JTAG operation, the input level of the RAM pins must conform to the device's DC specifications.

JTAG Port AC Test Conditions

Parameter	Symbol	Min	Unit
Input High/Low Level	V _{IH} /V _{IL}	1.3/0.5	V
Input Rise/Fall Time	T _R /T _F	1.0/1.0	ns
Input and Output Timing Reference Level	--	0.9	V

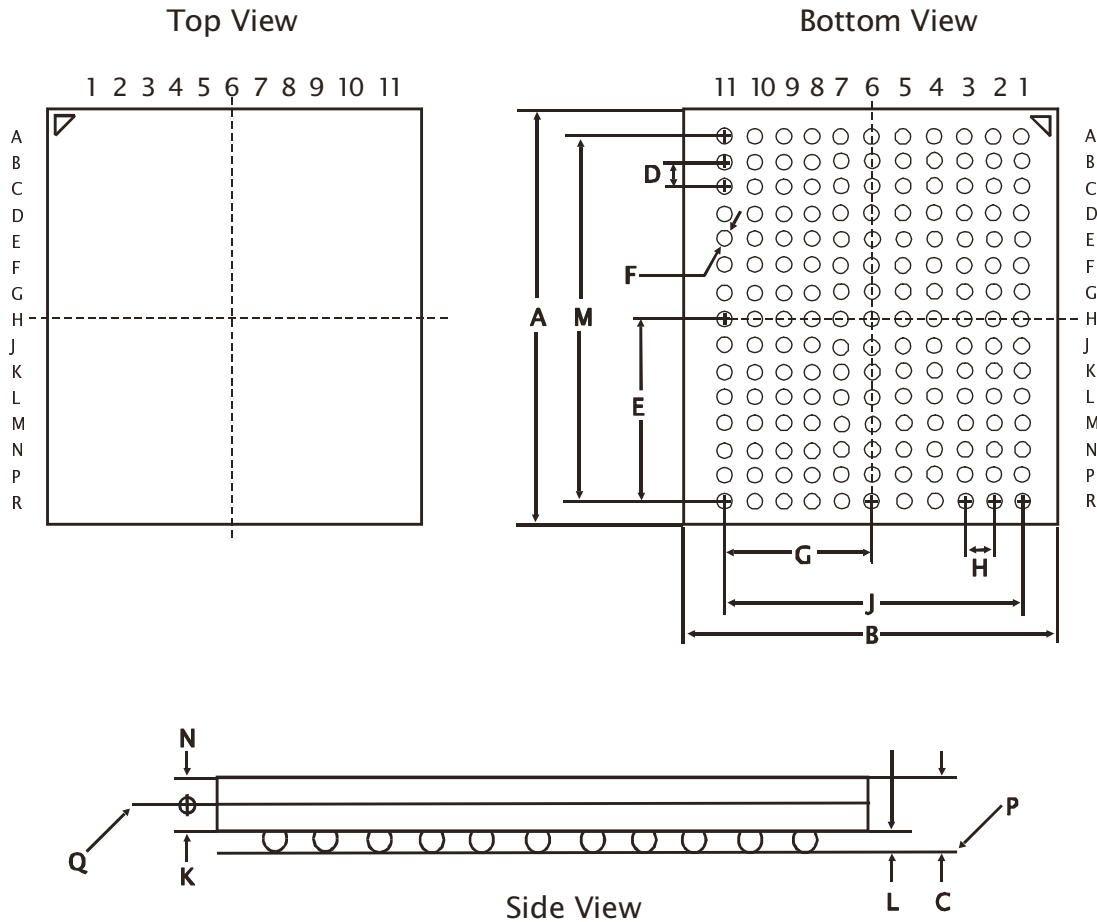
Parameters are measured with distributed scope and test jig capacitance. Conditions as shown in diagram below unless otherwise noted.



JTAG Port AC Electrical Characteristics (ns)

Parameter	Symbol	Min	Max
TCK Cycle Time	tTKC	50	—
TCK High Pulse Width	tTKH	20	—
TCK Low Pulse Width	tTKL	20	—
Set Up Time – (TDI, TMS, Capture)	tTS	5	—
Hold Time – (TDI, TMS, Capture)	tTH	5	—
TCK Low to TDO Valid	tTKQ	0	10

Package Drawing



Symbol	Description	Measurement (mm)
A	Chip Length	17.00±0.10
B	Chip Width	15.00±0.10
C	Chip Height	1.40 max.
D	Length between pin centers	1.00
E	Length between center pin and outermost pin	7.00
F	Pin diameter	0.50 +0.14 / -0.06
G	Width between center pin and outermost pin	5.00
H	Width between pin centers	1.00
J	Width between outermost pins	10.00
K	Height of circuit card	0.36
L	Height of pins	0.35±0.06

Symbol	Description	Measurement (mm)
M	Length between outermost pins	14.00
N	Height of encapsulant	0.53±0.05
P	Seating Plane *	
Q	Top Plane of circuit card **	

Pin centers: within 0.05 mm of relative position at MMC
Pin centers: within 0.25 mm of true position at MMC
Package length/width edges: uniform within 0.15 mm
Package weight: tbd
Solder pad type NSMD (non-solder mask defined)
JEDEC reference: MO-216 – design 4.6C

* Seating plane surface uniform within 0.15 mm

** Top plane parallel to seating plane within 0.25 mm

Document History

Datasheet for TSC4Q472U09 / 18 / 36

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1.0	23 May 2007	Original

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