72Mb Synchronous Double Transfer Rate (DTRII+™) 3T-iRAM™ With Common I/O, 2.5 Cycle Read Latency

Burst of 2 SRAM-Compatible

Features

- Error-resistant 3T-iRAM™ technology
- 300 to 400 MHz clock for high bandwidth
- Read latency of 2.5 clock cycles
- DTRII+™ Interface with Common I/O bus
- Fully pin-compatible with DDRII+ SRAMs
- JEDEC-standard pinout and package
- Burst of 2 Read and Write (Byte Writes)
- 1.8 V core power supply, 1.5 V I/O
- Synchronous internally self-timed Writes
- ZQ pin for programmable output drive strength
- QVLD pin indicates valid output data
- DLL for accurate data placement
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump 15mm x 17mm BGA, 1 mm bump pitch
- Pin-compatible with 9Mb, 18Mb, 36Mb, and 144Mb devices

Options / Marking

Options		Marking
Configurations:	8M x 9	S09
	4M x 18	S18
	2M x 36	S36
Package:	165 FBGA	B
Speed (MHz):	400 MHz	-400
	375 MHz	-375
	333 MHz	-333
	300 MHz	-300

Part number example: **TSC4D272E18B-333**

Functional Description

3T-iRAM™ is a unique type of dynamic memory. Tezzaron has crafted these pseudo-static devices to provide entirely SRAM-compatible interfaces and timing. The unique design of these 3T memories provides soft error rates up to 10 times lower than equivalent high-speed, high-density SRAMs.

DTRII+™ is a double transfer rate interface that is implemented with Common I/O architecture in these devices, making them drop-in compatible with DDRII+ SRAMs.

These synchronous pipelined 72Mb 3T-iRAM devices employ two register clocks, K and $\overline{K}$. These are independent single-ended clock inputs, not differential inputs. All synchronous inputs pass through registers controlled by the K clocks. Accesses are initiated on the rising edge of the positive clock and data is registered or driven on the rising edges of both clocks.

Write (input) and Read (output) data share the same data pins. Data outputs are tightly matched to two free-running echo clocks, CQ and $\overline{CQ}$, which are referenced with respect to the K clocks. Data inputs are controlled by self-timed Write circuitry.

These devices always transfer data in two packets. A0 is internally set to 0 for the first transfer of a data burst and automatically incremented to 1 for the second transfer.

Speed Parameter Synopsis:
(all units ns)

	-400	-375	-333	-300
tKHKH	2.50	2.66	3.00	3.30
tKHQV	0.45	0.45	0.45	0.45

Pin Configurations

2M x 36: Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{CQ}$	NC/144M	SA	R/$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{LD}$	SA	SA	CQ	A
B	NC	DQ27	DQ18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	NC	NC	DQ8	B
C	NC	NC	DQ28	VSS	SA	NC	SA	VSS	NC	DQ17	DQ7	C
D	NC	DQ29	DQ19	VSS	VSS	VSS	VSS	VSS	NC	NC	DQ16	D
E	NC	NC	DQ20	VDDQ	VSS	VSS	VSS	VDDQ	NC	DQ15	DQ6	E
F	NC	DQ30	DQ21	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ5	F
G	NC	DQ31	DQ22	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ14	G
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	DQ32	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ13	DQ4	J
K	NC	NC	DQ23	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ12	DQ3	K
L	NC	DQ33	DQ24	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2	L
M	NC	NC	DQ34	VSS	VSS	VSS	VSS	VSS	NC	DQ11	DQ1	M
N	NC	DQ35	DQ25	VSS	SA	SA	SA	VSS	NC	NC	DQ10	N
P	NC	NC	DQ26	SA	SA	QVLD	SA	SA	NC	DQ9	DQ0	P
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to DQ0:DQ8;
$\overline{BW1}$ controls writes to DQ9:DQ17;
$\overline{BW2}$ controls writes to DQ18:DQ26;
$\overline{BW3}$ controls writes to DQ27:DQ35.

4M x 18: Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NC	$\overline{LD}$	SA	SA	CQ	A
B	NC	DQ9	NC	SA	NC	K	$\overline{BW0}$	SA	NC	NC	DQ8	B
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ7	NC	C
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	D
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6	E
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5	F
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	G
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ	H
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC	J
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3	K
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2	L
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC	M
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC	N
P	NC	NC	DQ17	SA	SA	QVLD	SA	SA	NC	NC	DQ0	P
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17

8M x 9: Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{CQ}$	SA	SA	R/ $\overline{W}$	NC	$\overline{K}$	NC	$\overline{LD}$	SA	SA	CQ	A
B	NC	NC	NC	SA	NC	K	$\overline{BW0}$	SA	NC	NC	DQ3	B
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC	C
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	D
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2	E
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	F
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	G
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ	H
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC	J
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	K
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0	L
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	M
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC	N
P	NC	NC	DQ7	SA	SA	QVLD	SA	SA	NC	NC	DQ8	P
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI	R

Pin Descriptions

Symbol	Type	Description
SA	Input	Synchronous address inputs, both Read and Write
$\overline{LD}$	Input	Synchronous load; low initiates an access
NC	---	Not connected to die; can be tied to any voltage
R/ $\overline{W}$	Input	Read/Write select
$\overline{BW0}$ – $\overline{BW3}$	Input	Byte write controls
K / $\overline{K}$	Input	Input clocks (positive/negative)
TMS	Input	TAP: Test mode select
TDI	Input	TAP: Test data input
TCK	Input	TAP: Test clock
TDO	Output	TAP: Test data output
VREF	Input	HSTL input reference voltage
ZQ	Input	Output impedance matching; connect to Vss through a resistor or else tie to VDDQ
QVLD	Output	Valid Output Data indicator
DQx	I/O	Synchronous data signals for Write and Read
$\overline{Doff}$	Input	Disable DLL (when low) – affects device mode and timing! See DLL, page 7
CQ / $\overline{CQ}$	Output	Output echo clock (positive/negative)
VDD	Supply	Power supply to core; 1.8 V nominal
VDDQ	Supply	Isolated output buffer supply; 1.5 V nominal
VSS	Ground	Ground
NC/144M	--- / Input	For address expansion; can be tied to any voltage.

Functional Details

Clocks

K and $\overline{K}$ are the input clocks. All accesses are initiated on rising edges of K; rising edges of both clocks are used to capture synchronous inputs and to drive out data.

CQ and $\overline{CQ}$ are free-running echo clocks, generated by the RAM, that can be used to simplify data capture in high-speed systems. These clocks are referenced with respect to the K clocks.

Burst Operations

Read and write operations are synchronous pipelined "burst" operations. Every Read (or Write) command issues (or accepts) two beats of data in one clock cycle, executing data transfers on subsequent rising clock edges, as illustrated in the timing diagrams. It is not possible to stop a burst once it starts; two beats of data are always transferred.

Read Cycles

A Read access is initiated by asserting R/ $\overline{W}$ high and $\overline{LD}$ low on a rising edge of K and presenting the address to the SA pins at the same time. The address is stored in the Read address register. After two more rising edges of K, the RAM produces data out on the DQ pins in response to the next rising edge of $\overline{K}$. The second beat of data is transferred in response to the next rising edge of K, for a total of two transfers per address load. Read accesses may be initiated on every rising edge of K to produce a constant stream of output data timed by the rising edges of K and $\overline{K}$.

If all pending Read transactions are completed, internal circuitry tri-states the Q pins after the next rising edge of $\overline{K}$.

Write Cycles

A Write access is initiated by asserting both $\overline{\text{LD}}$ and R/$\overline{\text{W}}$ low on a rising edge of K and presenting the address on the SA pins at the same time. The address is stored in the Write address register. Data in is due at the device inputs on the next rising edge of K and on the subsequent rising edge of $\overline{\text{K}}$, for a total of two transfers per address load. Write accesses may be initiated on every rising edge of K to produce a constant stream of output data timed by the rising edges of K and $\overline{\text{K}}$.

Byte Write Control

Byte Write Enable pins are sampled at the same time that D pins are sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{\text{BW0}}$ controls D0–D8 inputs) inhibits the storage of that particular byte, leaving the data at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a two beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Example: x18 Write Sequence Using Byte Write Enables

Data In Sample Time	$\overline{\text{BW0}}$	$\overline{\text{BW1}}$	D0–D8	D9–D17
Beat 1	0	1	Data In	X
Beat 2	1	0	X	Data In

Resulting Write Operation:

Byte 1 D0–D8	Byte 2 D9–D17	Byte 3 D0–D8	Byte 4 D9–D17
Written	Unchanged	Unchanged	Written
Beat 1		Beat 2	

Notes: 1 = input high; 0 = input low; X = input "don't care".

Transitioning Between Read and Write Cycles

Read-to-Write transitions require the insertion of at least two NOP cycles; most applications may require a third NOP cycle to prevent contention.

Write-to-Read transitions do not require NOP cycles. If a Read is initiated immediately after a Write, the RAM prevents contention by performing a "posted" Write. The Write address and data are stored in registers until the next Write occurs. On the first Write cycle after the Read, the stored data is written before the new data.

Note: If a Read accesses the same address for which a Write has been posted, the Read bypasses the array and returns the data from the posted Write registers.

Output Driver Impedance Control

These devices are supplied with optional programmable impedance output drivers than can periodically readjust the impedance to compensate for drifts in supply voltage and temperature.

To enable this feature, the ZQ pin must be connected to Vss via an external resistor, RQ, with a value 5X the value of the intended RAM output impedance. The allowable range of RQ is between 175Ω and 350Ω. An internal calibration sequence occurs every 1024 cycles, and an update is performed during the next available deselected memory cycle.

To disable this feature, the ZQ pin may be tied directly to V_{DDQ}. The device then runs with a constant minimum impedance; no calibrations or adjustments are performed.

Valid Data Indicator (QVLD)

QVLD simplifies data capture on high-speed systems. The signal is generated along with Read (output) data, edge-aligned with the echo clock, and timed like a data pin. QVLD is asserted half a cycle before valid data appears.

Delay Lock Loop (DLL)

The DLL on these devices is designed to function between 120 MHz and the specified maximum clock frequency.
If the DLL is stopped by applying ground to $\overline{\text{Doff}}$, this device will behave in DDR mode instead of DDRII+ mode, and the timings shown in this data sheet will not apply.

The DLL may be reset by slowing or stopping the input clocks for a minimum of 30 ns. However, it is not necessary to reset the DLL in order to lock to the desired frequency; the DLL will relock after 2048 cycles of stable clock.

The DLL synchronizes to the K clock. This clock should have low phase jitter (see t_{KCVar} on page 12). If the incoming clock is not stabilized when DLL is enabled, the DLL may lock on the wrong frequency and cause undefined errors or failures during the initial stage. To avoid this, provide 2048 cycles of stable clock to allow DLL to relock.

Power-Up Sequence

These devices must be powered-up in a specific sequence in order to avoid undefined operations.

1. Power-up and maintain $\overline{\text{Doff}}$ at high state.

   1a. Apply VDD.

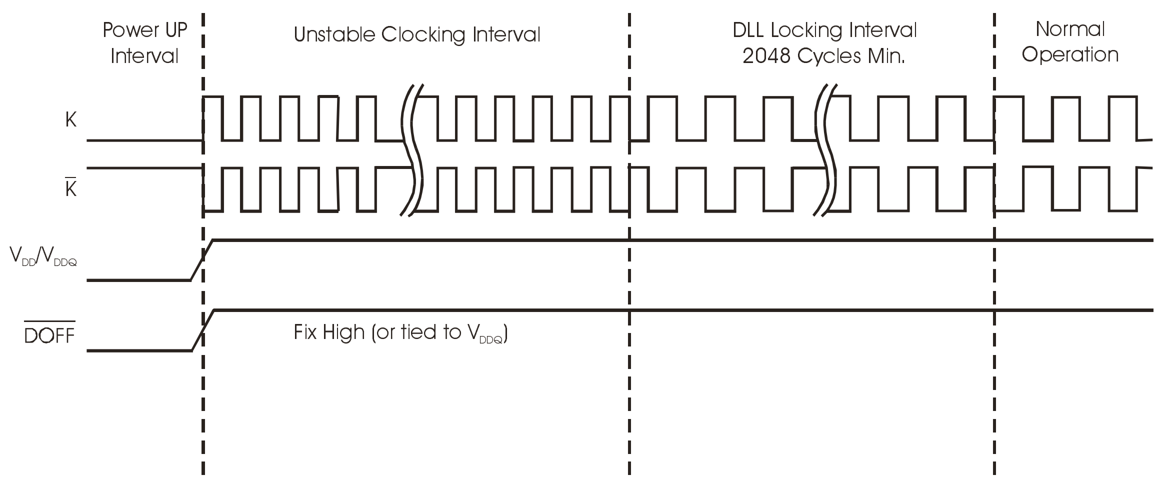
   1b. Apply VDDQ.

   1c. Apply VREF (may also be applied at the same time as VDDQ).

   Note: Clock starts when VDD and VDDQ are stable (< 0.1 V variance per 50ns).

2. After power is achieved and clocks K and $\overline{\text{K}}$ are stabilized, allow 2048 clock cycles to lock the DLL.

Power-Up Waveform



Truth Tables

I/O Truth Table

Function	K_n	$\overline{LD}$	$R/\overline{W}$	DQ	
Deselect (NOP)	↑	1	X	After Read accesses are complete, DQ = High-Z	
Write	↑	0	0	Data(A) at $K_{(n+1)}$↑	Data(A+1) at $\overline{K}_{(n+1)}$↑
Read	↑	0	1	Data(A) after $K_{(n+2)}$↑	Data(A+1) after $\overline{K}_{(n+2)}$↑

Notes: 1 = High, 0 = Low, X = Don't Care, ↑ = rising edge, A = latched address.

Byte Write Enable Truth Table, x18

$\overline{BW0}$	$\overline{BW1}$	DQ0 – DQ8	DQ9 – DQ17
1	1	X	X
0	1	Data	X
1	0	X	Data
0	0	Data	Data

Notes: 1 = High, 0 = Low, X = "Don't Care", Data = valid data to be written to device.

Byte Write Enable Truth Table, x36

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	DQ0 – DQ8	DQ9 – DQ17	DQ18 – DQ26	DQ27 – DQ35
1	1	1	1	X	X	X	X
0	1	1	1	Data	X	X	X
1	0	1	1	X	Data	X	X
0	0	1	1	Data	Data	X	X
1	1	0	1	X	X	Data	X
0	1	0	1	Data	X	Data	X
1	0	0	1	X	Data	Data	X
0	0	0	1	Data	Data	Data	X
1	1	1	0	X	X	X	Data
0	1	1	0	Data	X	X	Data
1	0	1	0	X	Data	X	Data
0	0	1	0	Data	Data	X	Data
1	1	0	0	X	X	Data	Data
0	1	0	0	Data	X	Data	Data
1	0	0	0	X	Data	Data	Data
0	0	0	0	Data	Data	Data	Data

Notes: 1 = High, 0 = Low, X = "Don't Care", Data = valid data to be written to device.

Electrical Characteristics

(All voltages reference to Vss)

Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Voltage: VDD pins	-0.5 to 2.9	V
VDDQ	Voltage: VDDQ pins	-0.5 to VDD	V
VREF	Voltage: VREF pins	-0.5 to VDDQ	V
VI/O	Voltage: I/O pins	–0.5 to VDDQ+0.3 (≤ 2.9 max.)	V
VIN	Voltage: other input pins	–0.5 to VDDQ+0.3 (≤ 2.9 max.)	V
	Static discharge voltage	>2001	V
IIN	Current: input on any pin	+/- 40	mA dc
IOUT	Current: output on any I/O pin	+/- 40	mA dc
	Latch-up current	>200	mA dc
TJ	Temperature: maximum junction	125	°C
TSTG	Temperature: storage	-65 to 150	°C
TA	Temperature: ambient (power applied)	-10 to 85	°C

Note: Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Extended exposure to conditions exceeding the Recommended Operating Conditions may affect reliability of this component.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	1.7	1.8	1.9	V
I/O Supply Voltage	VDDQ	1.4	1.5	1.6	V
Reference Voltage	VREF	0.68 *	0.75	0.85 *	V
Ambient Temperature (Commercial)	TA	0	25	70	°C
Ambient Temperature (Industrial)	TA	-40	25	85	°C

Notes: Unless otherwise noted, all performance specifications quoted are evaluated for worst case at 1.4 V ≤ VDDQ ≤ 1.6 V (i.e., 1.5 VI/O) and quoted at the worst case condition.

Power-up assumes: 1) linear ramp from 0V to VDD(MIN) within 200 ms
2) during ramp, VIH < VDD and VDDQ < VDD

Power supplies must be powered up simultaneously or else in the following sequence: VDD, VDDQ, VREF, followed by signal inputs. The power down sequence must be the reverse. VDDQ must not exceed VDD.

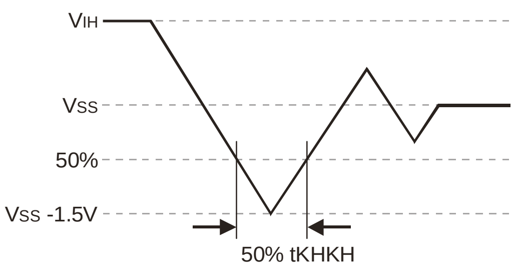
* VREF minimum is either 0.68 V or 0.46 * VDDQ , whichever is larger;
VREF maximum is either 0.85 V or 0.54 * VDDQ , whichever is smaller.

HSTL I/O Input Characteristics

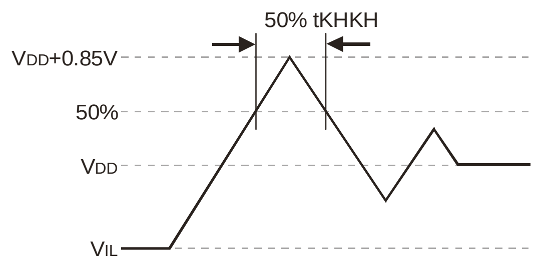
Parameter	Symbol	Min.	Max.	Unit	Notes
DC Input Logic High	V_{IH}(DC)	V_{REF} + 0.10	V_{DDQ} + 0.3	V	
DC Input Logic Low	V_{IL}(DC)	-0.3	V_{REF} – 0.10	V	
AC Input Logic High	V_{IH}(AC)	V_{REF} + 0.20	--	V	1
AC Input Logic Low	V_{IL}(AC)	--	V_{REF} – 0.20	V	1
V_{REF} Peak to Peak AC Voltage	V_{REF}(AC)	--	5% V_{REF}(DC)	V	2

1. To guarantee AC characteristics, V_{IL}, V_{IH}, Trise, and Tfall of inputs and clocks must be within 10% of each other.
2. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.

Undershoot/Overshoot Measurement and Timing



Undershoot



Overshoot

Capacitance

(T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V)
(These parameters tested initially and after any design or process change that may affect them)

Parameter (sample tested)	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF
Clock Capacitance	C_{CLK}	--	5	6	pF

Thermal Resistance

(These parameters tested initially and after any design or process change that may affect them)

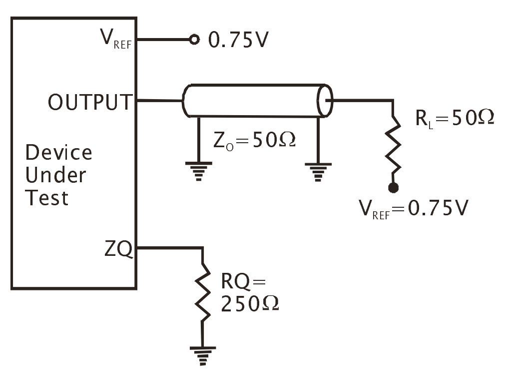
Parameter	Symbol	Test conditions	165 FBGA Package	Unit
Junction to Ambient	Θ_{JA}	Standard test methods and procedures for thermal impedance per EIA / JESD51	tbd	°C/W
Junction to Case	Θ_{JC}		tbd	°C/W

AC Test Conditions

Parameter	Conditions
Maximum input slew rate	2 V/ns
VDDQ	1.5 V
VREF	0.75 V
RQ	250Ω
Input reference level	VDDQ/2
Output reference level	VDDQ/2
Input pulse level (low)	0.25 V
Input pulse level (high)	1.25 V
Load	See diagrams below

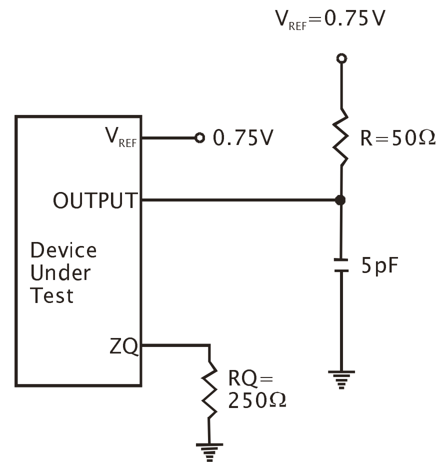
AC Test Load Diagrams

VDDQ = 1.5V



TEST CONFIGURATION “A”

Applies to all measurements unless specified otherwise.



TEST CONFIGURATION “B”

Output load as shown includes jig and scope.
Applies only to the measurement of tKHZ and tKLZ.

Input and Output Leakage Characteristics (μA)

Parameter	Symbol	Test Conditions	Min	Max
Input leakage current (except TAP pins)	IIZ	VIN = 0 to VDDQ	-2	2
Output leakage current	IOZ	Output disable, VOUT = 0 to VDDQ	-2	2

Switching Characteristics (ns)

Parameter	Symbol	-400		-375		-333		-300		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock/DLL										
K, $\overline{K}$ Clock Cycle Time	tKHKH	2.50	3.25	2.66	3.46	3.00	3.90	3.30	4.20	
K, $\overline{K}$ Clock High Pulse Width	tKHKL	1.00	--	1.06	--	1.20	--	1.32	--	
K, $\overline{K}$ Clock Low Pulse Width	tKLKH	1.00	--	1.06	--	1.20	--	1.32	--	
K to $\overline{K}$ High	$tKH\overline{KH}$	1.06	--	1.13	--	1.28	--	1.40	--	
K Static to DLL reset	tKCReset	30	--	30	--	30	--	30	--	3
tKC Variance (Clock phase jitter)	tKCVar	--	0.20	--	0.20	--	0.20	--	0.20	2
Output Times										
K, $\overline{K}$ Clock High to Data Output Valid	tKHQV	--	0.45	--	0.45	--	0.45	--	0.45	
K, $\overline{K}$ Clock High to Data Output Hold	tKHQX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	
K, $\overline{K}$ Clock High to Echo Clock Valid	tKHCQV	--	0.45	--	0.45	--	0.45	--	0.45	
K, $\overline{K}$ Clock High to Echo Clock Hold	tKHCQX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	
CQ, $\overline{CQ}$ High to Output Data Valid	tCQHQV	--	0.20	--	0.20	--	0.20	--	0.20	
CQ, $\overline{CQ}$ High to Output Data Invalid	tCQHQX	0.20	--	0.20	--	0.20	--	0.20	--	
CQ, $\overline{CQ}$ High Pulse Width	tCQHCHL	0.81	--	0.88	--	1.03	--	1.15	--	4
CQ High to $\overline{CQ}$ HIGH	$tCQH\overline{CQH}$	0.81	--	0.88	--	1.03	--	1.15	--	4
K Clock High to Data Output High-Z	tKHZ	--	0.45	--	0.45	--	0.45	--	0.45	1
K Clock High to Data Output Low-Z	tKLZ	-0.45	--	-0.45	--	-0.45	--	-0.45	--	1
CQ, $\overline{CQ}$ High to QVLD Valid	tQVLD	-0.20	0.20	-0.20	0.20	-0.20	0.20	-0.20	0.20	5
Input Times										
Address Valid to K Rising Edge	tAVKH	0.40	--	0.40	--	0.40	--	0.40	--	
R/$\overline{W}$, $\overline{LD}$ Valid to K Rising Edge	tIVKH	0.40	--	0.40	--	0.40	--	0.40	--	
DQx, $\overline{BWx}$ Valid to K Rising Edge	tDVKH	0.28	--	0.28	--	0.28	--	0.28	--	
K Rising Edge to Address Hold	tKHAX	0.40	--	0.40	--	0.40	--	0.40	--	
K Rising Edge to R/$\overline{W}$, $\overline{LD}$ Hold	tKHIX	0.40	--	0.40	--	0.40	--	0.40	--	
K, $\overline{K}$ Rising Edge to DQx, $\overline{BWx}$ Hold	tKHDX	0.28	--	0.28	--	0.28	--	0.28	--	

Notes:

A part follows the input/output timings of the frequency at which it is being operated, regardless of its speed rating.

DLL Lock Time (tKClock) is a minimum of 2048 cycles in all cases. V_{DD} slew rate must be less than 0.1 V DC per 50ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.

1. At any given voltage and temperature tKLZ > tKHZ and tKHZ < tKHQV.
   These parameters are tested in "Configuration B" (see page 11).
2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
3. Hold to > V_{IH} or < V_{IL}.
4. These parameters are extrapolated from input timing parameters as $tKH\overline{KH}$ minus internal jitter of 250 picosec. Note that tKCVar is already included in $tKH\overline{KH}$. These parameters are guaranteed by design, not tested in production.
5. Timing applies to both rising and falling edges of QVLD.

Programmable Impedance HSTL Output Driver DC Electrical Characteristics (V)

Parameter	Symbol	Condition	Min	Max
Output High Voltage	V_{OH}	Outputs are impedance controlled. 175Ω ≤ RQ ≤ 350Ω I_{OH} = – (V_{DDQ}/2) / (RQ/5) +/– 15%	V_{DDQ}/2 – 0.12	V_{DDQ}/2 + 0.12
		I_{OH} = –1.0 mA, nominal impedance Minimum Impedance mode, ZQ = V_{DDQ}	V_{DDQ} – 0.2	V_{DDQ}
Output Low Voltage	V_{OL}	Outputs are impedance controlled. 175Ω ≤ RQ ≤ 350Ω I_{OL} = (V_{DDQ}/2) / (RQ/5) +/– 15%	V_{QQD}/2 – 0.12	V_{DDQ}/2 + 0.12
		I_{OL} = 1.0 mA, nominal impedance Minimum Impedance mode, ZQ = V_{DDQ}	V_{SS}	0.2

Operating Currents (DDR)

Parameter	Test Conditions	Symbol	-333		-300		-267	
			Min	Max	Min	Max	Min	Max
x36 Operating Current	V_{DD} = max, I_{OUT} = 0 mA, f = max	I_{DD}	tbd	tbd	tbd	tbd	tbd	tbd
x18 Operating Current			tbd	tbd	tbd	tbd	tbd	tbd
x9 Operating Current			tbd	tbd	tbd	tbd	tbd	tbd
Standby Current (NOP)	Device deselected, V_{DD} = max, I_{OUT} = 0 mA, f = max, Inputs ≤ 0.2 V or ≥ V_{DD} – 0.2V	I_{SB1}	tbd	tbd	tbd	tbd	tbd	tbd

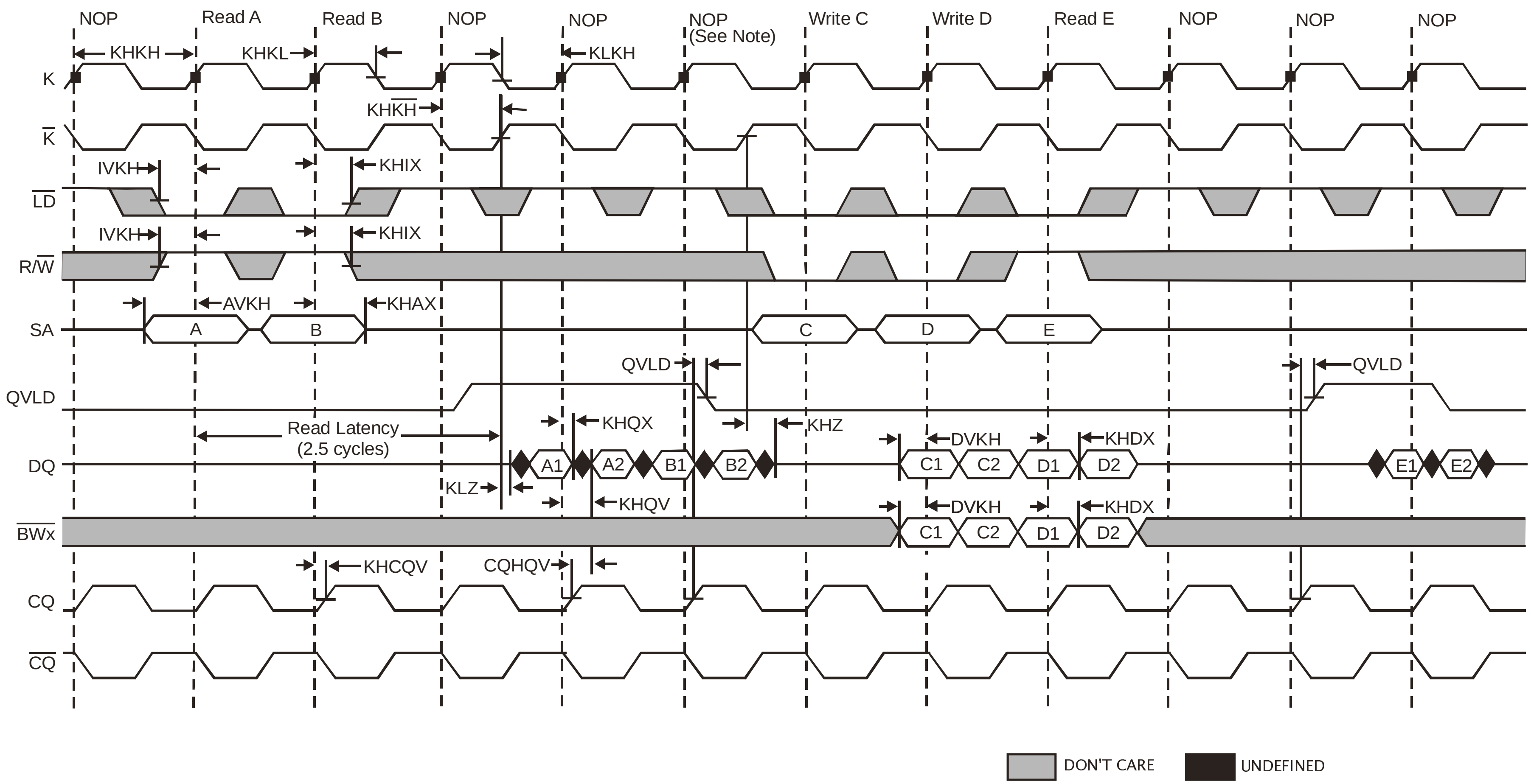
Notes:

Power is measured with output pins floating.

Operating current is calculated with 50% read cycles and 50% write cycles.

Standby Current applies only after all pending read and write burst operations are completed.

Timing Diagram – Read, Write, NOP



Notes: Two NOP cycles are mandatory between Read and Write; a third NOP is usually required to prevent bus contention.
Outputs are disabled (High-Z) 2.5 cycles after a NOP.

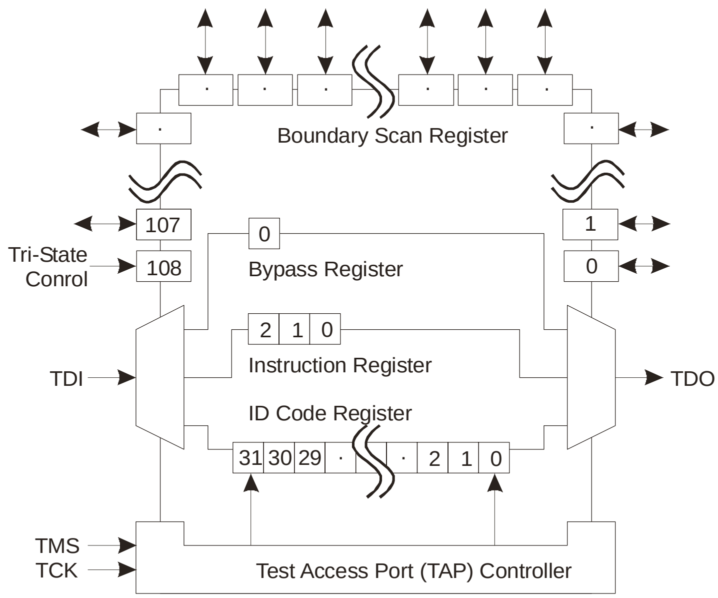
JTAG Port Operation

Overview

This device incorporates a serial boundary scan interface that complies with IEEE Standard 1149.1-1990, commonly known as JTAG. The JTAG Port is also known as a Test Access Port, or TAP. It can be used to read the device ID code, monitor all RAM input and I/O pads, drive pre-loaded values into the I/O bus, or the I/O bus to a High-Z state.

The port's input interface levels scale with V_{DD} and the output drivers are powered by V_{DDQ}. The port is reset at power-up and remains inactive until clocked. Pins, registers, states, and instructions are described below.

JTAG Test Access Port Block Diagram



JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all events. Inputs are captured on the rising edge; outputs are driven on the falling edge.
TMS	Test Mode Select	In	Command input for the JTAG state machine, sampled on the rising edge of TCK.
TDI	Test Data In	In	The input side of any selected register, sampled on the rising edge of TCK.
TDO	Test Data Out	Out	The output side of any selected register, driven on the falling edge of TCK.

Notes: TCK, TDI, and TMS have internal pull-up circuits; when undriven they produce a logic one input level.

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The JTAG controller is reset automatically at power-up, and again whenever it enters the Test-Logic-Reset state.

The "selected" register is determined by the current instruction and the state of the JTAG controller.

Disabling the JTAG Port

For normal operation of the device without using JTAG, the controller can be held in a permanent Reset state. To do this, TCK, TDI, and TMS are left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Registers

The JTAG interface has four serial shift registers that are used in conjunction with JTAG instructions. When a register is selected, it is placed between TDI and TDO so that it can shift data out serially on the falling edges of TCK and capture input data on the rising edges of TCK, depending on the state of the controller.

Instruction Register

The three-bit Instruction Register holds an instruction to be executed. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller enters the Test-Logic-Reset state. The user may load instructions through the TDI pin using the various IR (Instruction Register) states. The Instruction Register is always selected in the IR states, regardless of the current instruction.

Bypass Register

The single-bit Bypass Register can be placed between TDI and TDO to pass serial data through the JTAG Port with as little delay as possible. The Bypass Register is selected by the BYPASS instruction.

Identification (ID) Register

The 32-bit ID Register receives an identification code from an on-chip ID ROM. The code describes various attributes of the RAM as indicated in the table below. The ID Register is selected by the IDCODE instruction.

ID Code Contents

	Die Revision Code				Not Used								I/O Configuration								Tezzaron Semiconductor JEDEC Vendor ID Code											Presence Register
Bit#	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
x36	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1
x16	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0	1
x9	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0	0	1	0	1	1	0	0	1

Boundary Scan Register

The Boundary Scan Register is a chain of 109 cells. Each cell contains a Scan bit and an Update bit. The Scan bits can capture the logic level found on the RAM's I/O pins; the Update bits can drive a preloaded set of data onto the RAM's outputs. The Boundary Scan Register cells are daisy chained together so their contents can be shifted out serially through the TDO pin and loaded through the TDI pin. The relationship between the device pins and the cells in the Boundary Scan Register is described in the Scan Order Table below; note that the register includes a number of special purpose cells that do not represent I/O pins. The Boundary Scan Register is selected by the SAMPLE-Z, SAMPLE/PRELOAD, and EXTEST instructions.

Scan Order Table

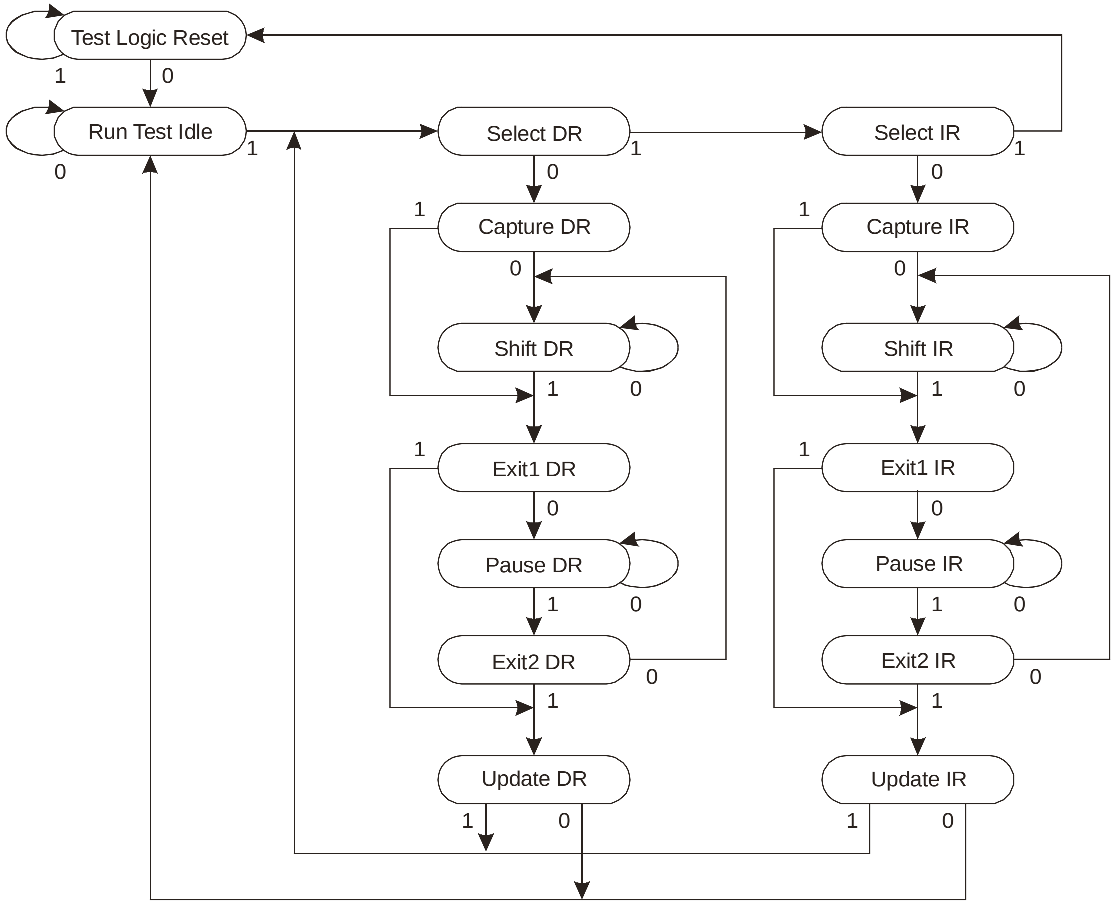
Cell#	Pin Name	I/O	Notes
0	tbd	tbd	
1	tbd	tbd	
2	tbd	tbd	
3	tbd	tbd	
4	tbd	tbd	
5	tbd	tbd	
6	tbd	tbd	
7	tbd	tbd	
8	tbd	tbd	
9	tbd	tbd	
10	tbd	tbd	
11	tbd	tbd	
12	tbd	tbd	
13	tbd	tbd	
14	tbd	tbd	
15	tbd	tbd	
16	tbd	tbd	
17	tbd	tbd	
18	tbd	tbd	
19	tbd	tbd	
20	tbd	tbd	
21	tbd	tbd	
22	tbd	tbd	
23	tbd	tbd	
24	tbd	tbd	
25	tbd	tbd	
26	tbd	tbd	
27	tbd	tbd	

Cell#	Pin Name	I/O	Notes
28	tbd	tbd	
29	tbd	tbd	
30	tbd	tbd	
31	tbd	tbd	
32	tbd	tbd	
33	tbd	tbd	
34	tbd	tbd	
35	tbd	tbd	
36	tbd	tbd	
37	tbd	tbd	
38	tbd	tbd	
39	tbd	tbd	
40	tbd	tbd	
41	tbd	tbd	
42	tbd	tbd	
43	tbd	tbd	
44	tbd	tbd	
45	tbd	tbd	
46	tbd	tbd	
47	tbd	tbd	
48	tbd	tbd	
49	tbd	tbd	
50	tbd	tbd	
51	tbd	tbd	
52	tbd	tbd	
53	tbd	tbd	
54	tbd	tbd	
55	tbd	tbd	

Cell#	Pin Name	I/O	Notes
56	tbd	tbd	
57	tbd	tbd	
58	tbd	tbd	
59	tbd	tbd	
60	tbd	tbd	
61	tbd	tbd	
62	tbd	tbd	
63	tbd	tbd	
64	tbd	tbd	
65	tbd	tbd	
66	tbd	tbd	
67	tbd	tbd	
68	tbd	tbd	
69	tbd	tbd	
70	tbd	tbd	
71	tbd	tbd	
72	tbd	tbd	
73	tbd	tbd	
74	tbd	tbd	
75	tbd	tbd	
76	tbd	tbd	
77	tbd	tbd	
78	tbd	tbd	
79	tbd	tbd	
80	tbd	tbd	
81	tbd	tbd	
82	tbd	tbd	
83	tbd	tbd	

Cell#	Pin Name	I/O	Notes
84	tbd	tbd	
85	tbd	tbd	
86	tbd	tbd	
87	tbd	tbd	
88	tbd	tbd	
89	tbd	tbd	
90	tbd	tbd	
91	tbd	tbd	
92	tbd	tbd	
93	tbd	tbd	
94	tbd	tbd	
95	tbd	tbd	
96	tbd	tbd	
97	tbd	tbd	
98	tbd	tbd	
99	tbd	tbd	
100	tbd	tbd	
101	tbd	tbd	
102	tbd	tbd	
103	tbd	tbd	
104	tbd	tbd	
105	tbd	tbd	
106	tbd	tbd	
107	tbd	tbd	
108	Tri-State Control	n/a	

JTAG Controller State Diagram



JTAG Controller States

Overview

The JTAG controller is inactive until clocked with TCK. When TCK is activated, the controller is in the Test Logic Reset state. Subsequent transitions between states are controlled by the TMS signal as shown in the diagram above. TMS is sampled at each rising edge of TCK.

The DR states select and manipulate the four JTAG data registers; the IR states select and manipulate the Instruction Register.

Test Logic Reset

In this state, the IDCODE instruction is loaded into the Instruction Register, no control is exerted over the RAM's output pins, and the RAM executes as if the JTAG port were disabled. If TMS is held at 1 for five cycles, the controller returns to this state and loops until it detects a TMS value of 0.

Run Test Idle

This is the entry point for all instructions. The controller can loop here as needed, but performs no functions.

Select DR

The controller selects a data register (determined by the current instruction) and places it between TDI and TDO.

Capture DR

Depending upon the current instruction, the selected register may receive data from sources other than TDI.

Shift DR

On the falling edge of TCK, the least significant bit of the selected register is shifted onto TDO. On the rising edge of TCK, the value on the TDI pin is captured and shifted into the most significant bit of the selected register.

Exit1 DR

Data movement stops. No function is performed.

Pause DR

The controller can loop here, but performs no functions.

Exit2 DR

No function is performed.

Update DR

If the current instruction is SAMPLE or EXTEST, data in the Boundary Scan Register is copied from the Scan bits to the Update bits. Otherwise, no function is performed.

Select IR

The Instruction Register is selected and placed between TDI and TDO.

Capture IR

The controller loads the two least significant bits of the Instruction Register with 01.

Shift IR, Exit1 IR, Pause IR, Exit2 IR

These states are analogous to Shift DR, Exit1 DR, Pause DR, and Exit2 DR.

Update IR

Instruction loading is complete; the instruction is decoded for implementation. If the new instruction is EXTEST or SAMPLE-Z, JTAG exerts control over the RAM's output pins; otherwise, it releases control of those pins.

JTAG Controller Instruction Set

Instruction Summary

Instruction	Binary Code	Description
EXTEST	000	Either drives contents onto RAM outputs or forces outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
IDCODE	001	Selects and loads ID Register; allows reading of register. **Default instruction** – automatically loaded in test-logic-reset state.
SAMPLE-Z	010	Forces all RAM outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading of Boundary Scan Register.
RFU	011	Do not use this instruction; reserved for future use. (Currently replicates BYPASS instruction.)
SAMPLE/PRELOAD	100	Selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
TEZZARON	101	Tezzaron private instruction; do not use.
RFU	110	Do not use this instruction; Reserved for Future Use. (Currently replicates BYPASS instruction.)
BYPASS	111	Selects Bypass Register; allows rapid pass-through of data.

Instruction Descriptions

NOTE: Several of these instructions capture signals from the RAM's I/O ring. The user must be aware that the JTAG clock (TCK) operates at 20 MHz or less, while the RAM clock operates more than an order of magnitude faster. Because of the difference in clock frequencies, it is possible that an input or output will undergo a transition during the capture. In this case, the signal may be captured while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured, and repeatable results may not be possible. To guarantee that the correct value of a signal is captured, the signal must be stabilized long enough to meet the JTAG set-up plus hold times (tTS + tTH). If there is no way in a design to stop (or slow) the RAM clock, the RAM clock inputs might not be captured correctly; however, it is still possible to capture all other signals and simply ignore the captured values of the RAM clock signals.

BYPASS

This instruction allows test data to pass through the device with minimal delay, to facilitate testing of other devices on the scan path.

Select-DR: The Bypass Register is placed between TDI and TDO.

Shift-DR: Data is shifted out through TDO and in from TDI.

SAMPLE/PRELOAD

This instruction allows sample data to be captured and examined without interfering with normal device operation. It also allows test data to be pre-loaded for later use with the EXTEST instruction.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data from the Scan bits is copied into the Update bits for later use (see EXTEST).

EXTEST

This instruction captures sample data and sets up test data, much like SAMPLE/PRELOAD, but it also controls the RAM's output pins. EXTEST is for testing only, as it will disrupt normal operation of the device. As soon as the EXTEST instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded. The values in the Boundary Scan Register's Update bits are driven onto the output pins, *unless the Tri-State Control cell has been set (see below)*, in which case the output pins are tri-stated.

EXTEST and Tri-State

The Boundary Scan Register's last cell, #108, is the Tri-State Control cell. During EXTEST, it directly controls the state of the RAM's output pins. When HIGH, it enables the Update bit values to drive the output bus; when LOW, it places the output bus into a High-Z condition. The Tri-State Control cell's value is set to HIGH whenever the controller is in the "Test-Logic-Reset" state. The value is changed with the SAMPLE/PRELOAD or EXTEST instruction by shifting the desired value into the cell during the Shift-DR state. During Update-DR, the new value is copied into the cell's Update bit. From there, it controls the EXTEST instruction's behavior.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data in the Scan bits is copied to the Update bits. The values take effect immediately, driving the RAM's output bus as directed.

IDCODE

IDCODE is the default instruction, loaded automatically whenever the controller is placed in the Test-Logic-Reset state. It allows access to the device's internal ID ROM contents.

Select-DR: The ID Register is placed between TDI and TDO.

Capture-DR: The ID Register is loaded with the device's 32-bit identification code from the ID ROM.

Shift-DR: The contents of the ID Register is shifted out through TDO.

SAMPLE-Z

This instruction functions somewhat like EXTEST, except that the output bus is always tri-stated and the Update bits are not changed. Like EXTEST, it is disruptive to normal device operation. As soon as the SAMPLE-Z instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded.

Select-DR: The Boundary Scan Register is connected between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits.

Shift-DR: Data in the Scan bits is shifted out serially through TDO.

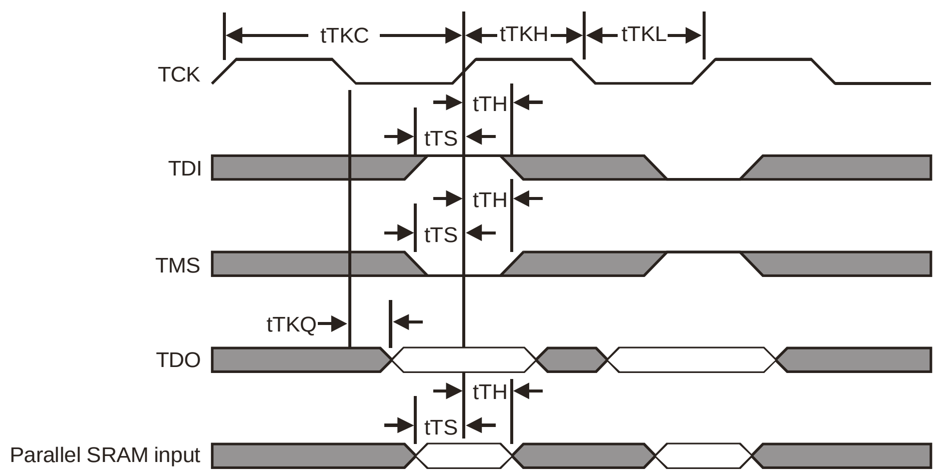
Tezzaron

This instruction is reserved for vendor use; do not use.

RFU

This instruction is reserved for future use; in this device it replicates the BYPASS instruction.

JTAG Port Timing Diagram



JTAG Port Recommended Operating Conditions and DC Characteristics (V)

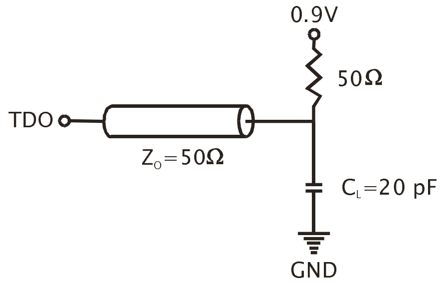
Parameter	Symbol	Min.	Typ.	Max.
Power Supply Voltage	V_{DDQ}	1.7	1.8	1.9
Input High Voltage	V_{IH}	1.3	--	V_{DD} + 0.3
Input Low Voltage	V_{IL}	–0.3	--	0.5
Output High Voltage (I_{OH} = -2 mA)	V_{OH}	1.4	--	V_{DD}
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	V_{SS}	--	0.4

Note: During JTAG operation, the input level of the RAM pins must conform to the device's DC specifications.

JTAG Port AC Test Conditions

Parameter	Symbol	Min	Unit
Input High/Low Level	V_{IH}/V_{IL}	1.3/0.5	V
Input Rise/Fall Time	TR/TF	1.0/1.0	ns
Input and Output Timing Reference Level	--	0.9	V

Parameters are measured with distributed scope and test jig capacitance.
Conditions as shown in diagram below unless otherwise noted.

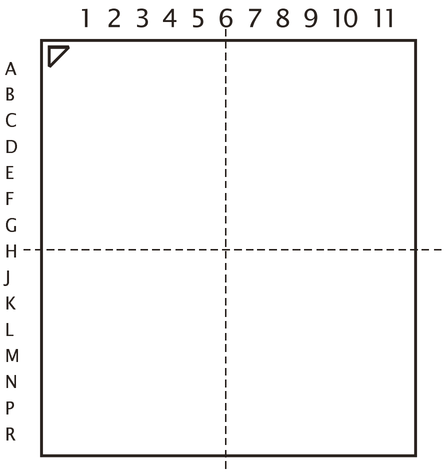


JTAG Port AC Electrical Characteristics (ns)

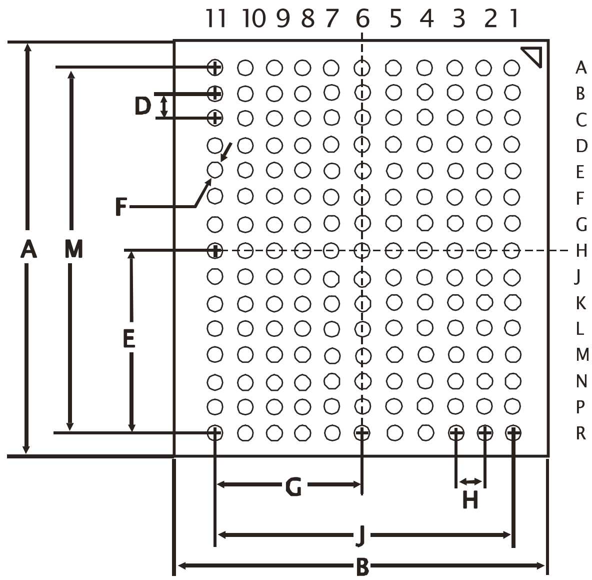
Parameter	Symbol	Min	Max
TCK Cycle Time	tTKC	50	—
TCK High Pulse Width	tTKH	20	—
TCK Low Pulse Width	tTKL	20	—
Set Up Time – (TDI, TMS, Capture)	tTS	5	—
Hold Time – (TDI, TMS, Capture)	tTH	5	—
TCK Low to TDO Valid	tTKQ	0	10

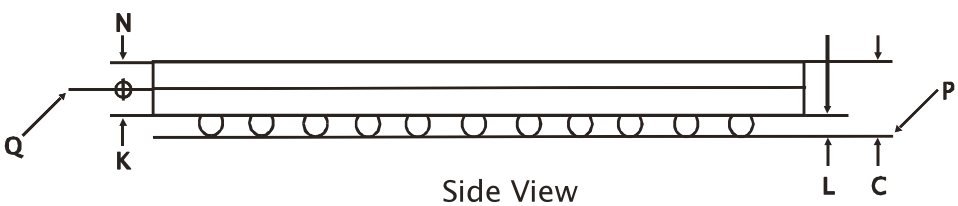
Package Drawing

Top View



Bottom View





Side View

Symbol	Description	Measurement (mm)
A	Chip Length	17.00±0.10
B	Chip Width	15.00±0.10
C	Chip Height	1.40 max.
D	Length between pin centers	1.00
E	Length between center pin and outermost pin	7.00
F	Pin diameter	0.50 +0.14 / -0.06
G	Width between center pin and outermost pin	5.00
H	Width between pin centers	1.00
J	Width between outermost pins	10.00
K	Height of circuit card	0.36
L	Height of pins	0.35±0.06

Symbol	Description	Measurement (mm)
M	Length between outermost pins	14.00
N	Height of encapsulant	0.53±0.05
P	Seating Plane *	
Q	Top Plane of circuit card **	

Pin centers: within 0.05 mm of relative position at MMC
Pin centers: within 0.25 mm of true position at MMC
Package length/width edges: uniform within 0.15 mm
Package weight: tbd
Solder pad type NSMD (non-solder mask defined)
JEDEC reference: MO-216 – design 4.6C

* Seating plane surface uniform within 0.15 mm
** Top plane parallel to seating plane within 0.25 mm

Document History

Datasheet for TSC4D272E09 / 18 / 36

Revision	Date	Changes
1.0	12 February 2007	Original

Document Contents

